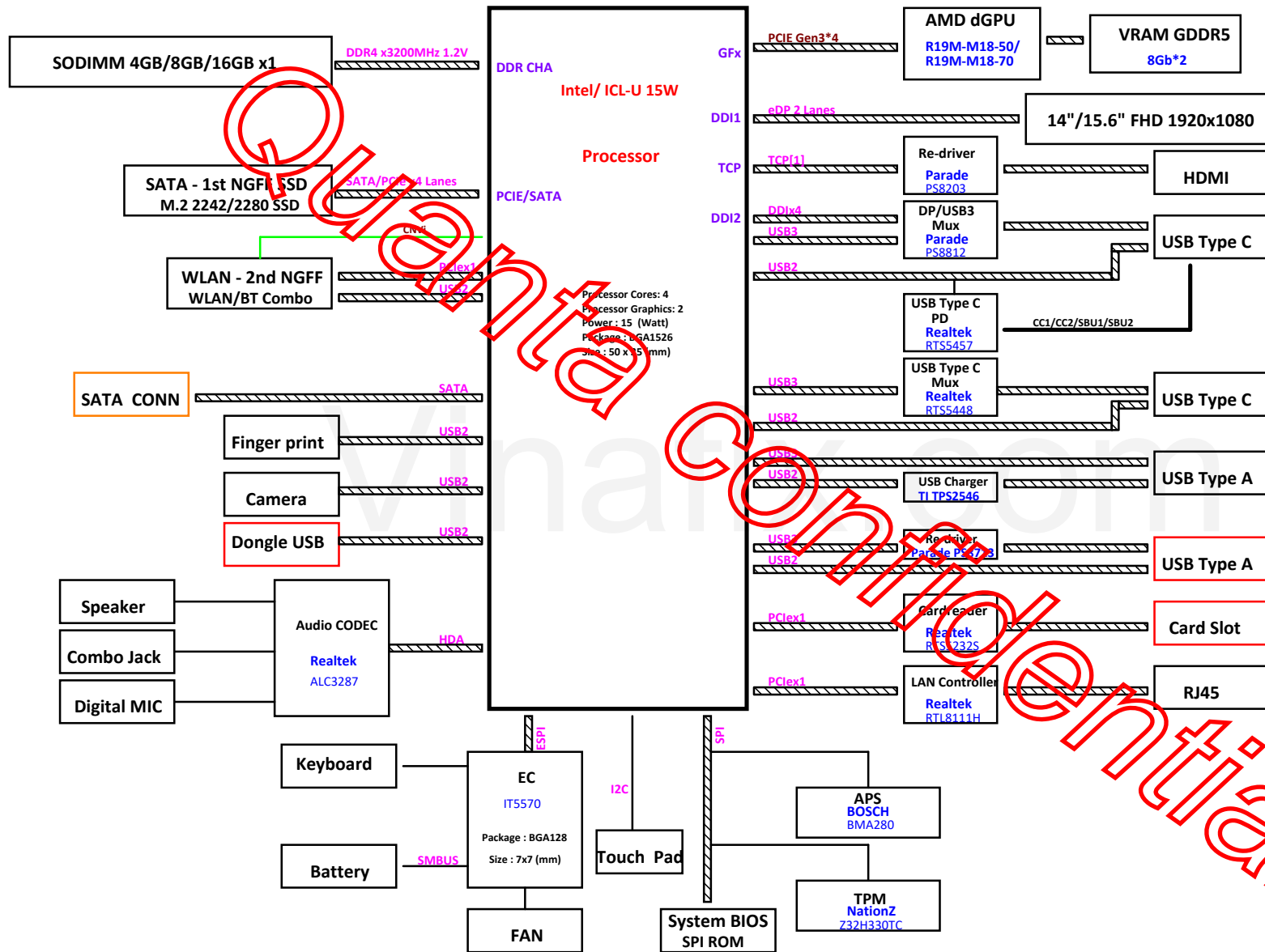
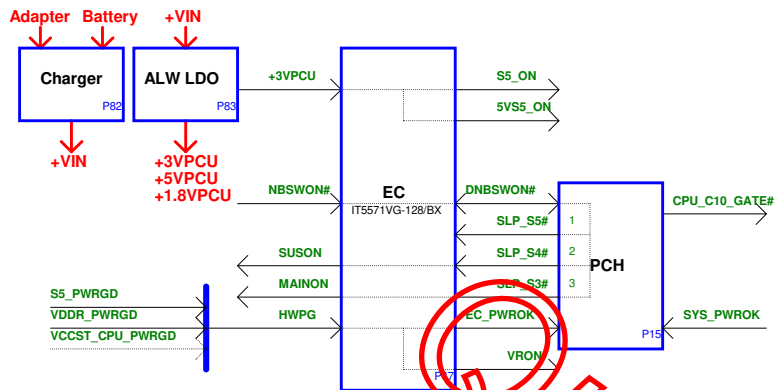


Lenovo V340 14"/15.6" Notebook Intel ICE Lake U Block Diagram



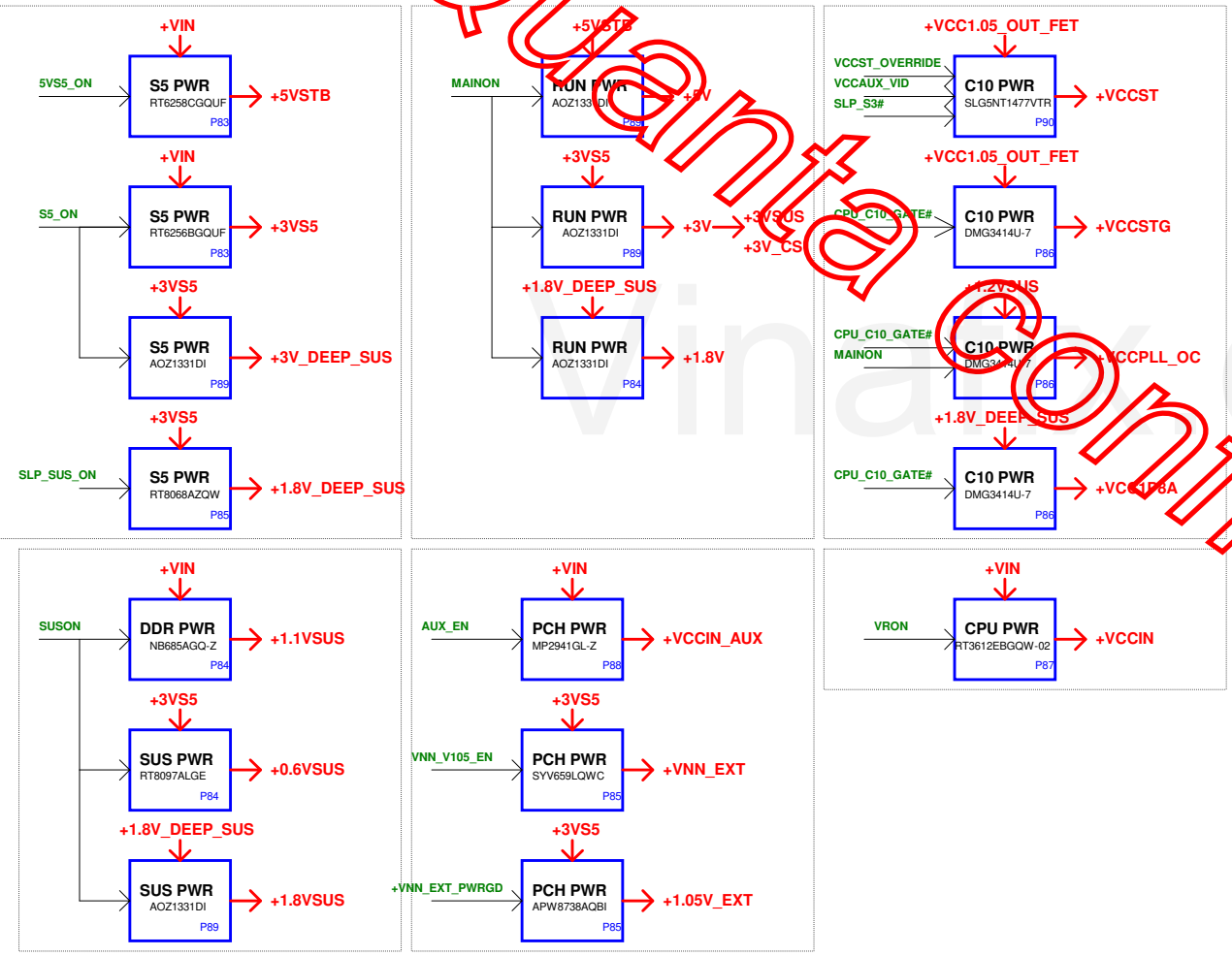
PCB 10L STACK UP

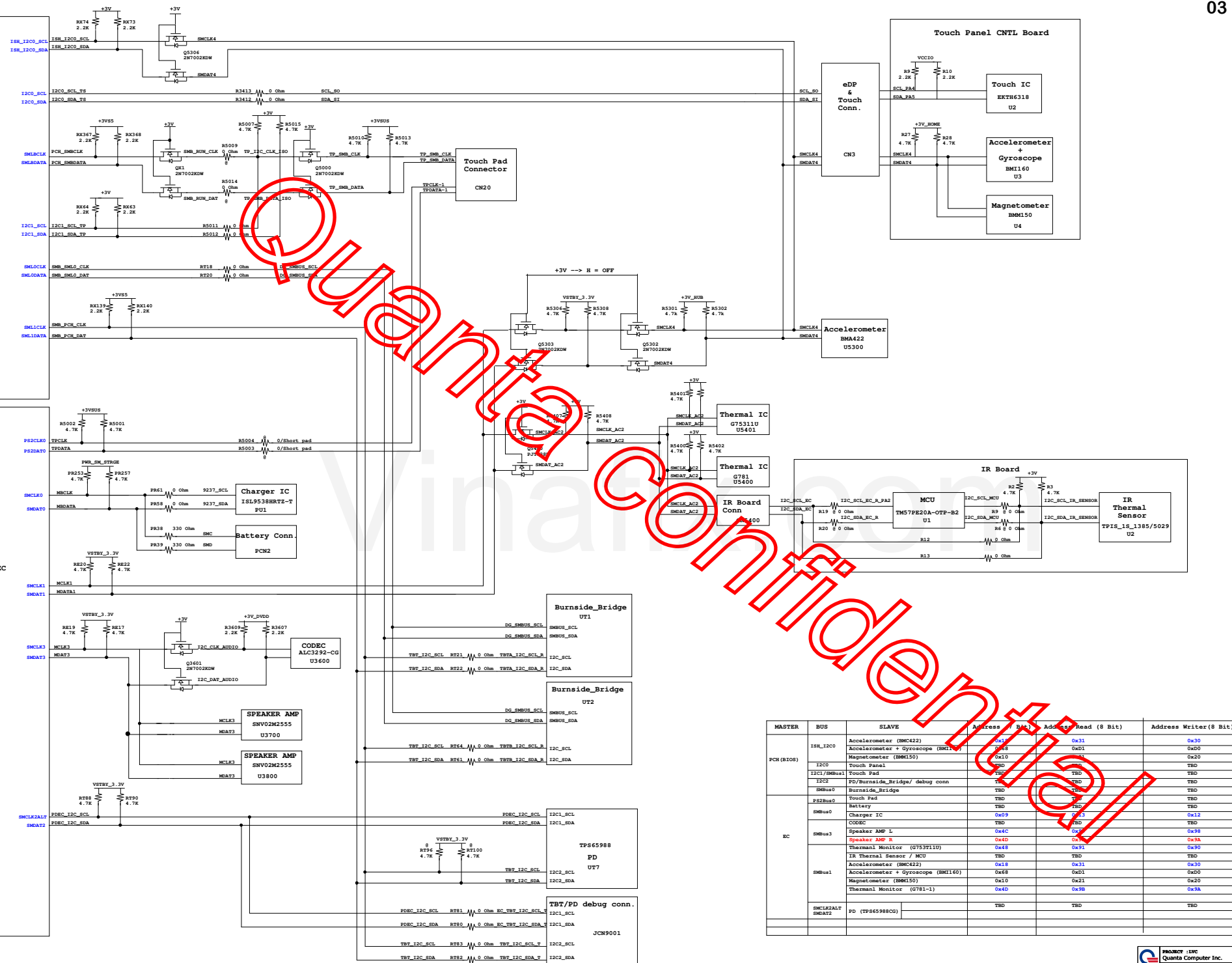
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(High)
LAYER 5 : SGND
LAYER 6 : SVCC
LAYER 7 : IN3
LAYER 8 : IN4(High)
LAYER 9 : SGND
LAYER 10 : BOT



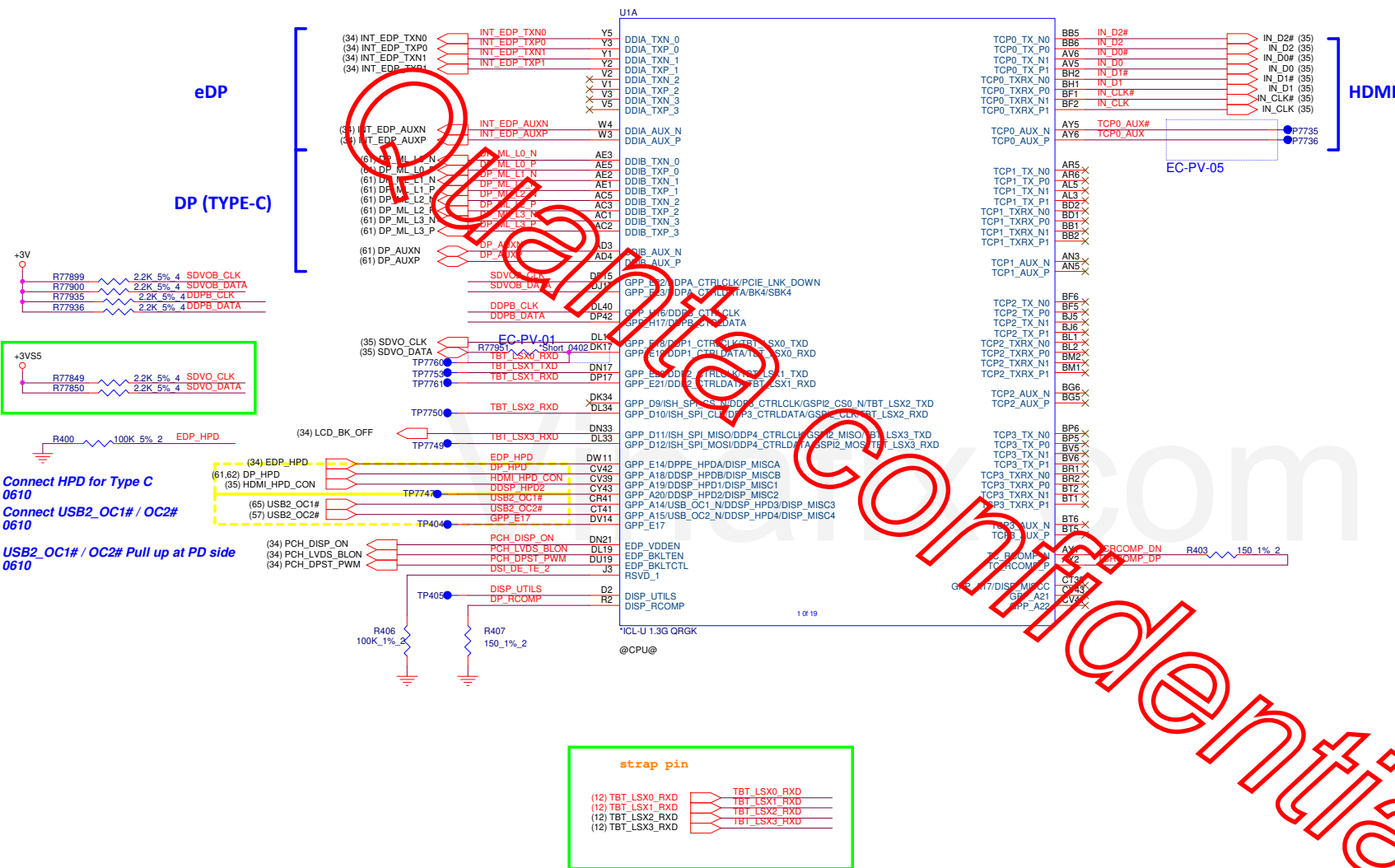
Main Power Rails

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+3V_WLAN_P	+3.3V	WLAN Power	CNVI_EN#	
+1.8VSUS	+1.8V	LPDDR4/4X Suspend Power	SUSON	
+0.6VSUS	+0.6V	LPDDR4/4X Suspend Power	SUSON	
+1.05V_EXT	+1.05V	PCH Power	+VNN_EXT_PWRGD	
+VNN_EXT	+1.05V	PCH Power	VNN_V105_EN	
+1.1VSUS	+1.1V	LPDDR4/4X Suspend Power	SUSON	
+1.8V	+1.8V	Audio Codec power	MAINON	
+1.8V_DEEP_SUS	+1.8V	PCH power	SLP_SUS_ON	
+3V	+3.3V	3V Run Power	MAINON	
+3VSUS	+3.3V	3V Suspend Power	MAINON	
+3VS5	+3.3V	3V S5 Power	S5_ON	
+3VPCU	+3.3V	3V Always Power	+VIN	
+5V	+5V	5V Run Power	MAINON	
+5VSTB	+5V	5V S5 Power	5VS5_ON	
+5VPCU	+5V	5V Always Power	+VIN	
+VCCIN_AUX	+1.8V	PCH Power	AUX_EN	
+VCCIN	SVID +1.89V(MAX)	CPU Core Power	VRON	
+VIN	+19V	AC power input		





MASTER	BUS	SLAVE	Address	Bit	Address Head (8 Bit)	Address Writer (8 Bit)
PCH (BIOS)	ISA_12C0	Accelerometer (BMA422)	0x10	0x31	0x31	0x30
		Accelerometer + Gyroscope (BMI160)	0x10	0x01	0x01	0x00
		Magnetometer (BMI150)	0x10	0x01	0x01	0x00
	12C0	Touch Panel	0x10	0x01	0x01	0x00
	12C1/BMBus1	Touch Pad	0x10	0x01	0x01	0x00
	12C2	TP/Burnside Bridge/ debug conn	0x10	0x01	0x01	0x00
EC	SMBus0	Burnside Bridge	0x10	0x01	0x01	0x00
	P22Bus0	Touch Pad	0x10	0x01	0x01	0x00
	SMBus0	Battery	0x10	0x01	0x01	0x00
	SMBus0	Charger IC	0x10	0x01	0x01	0x00
	CODEC	CODEC	0x10	0x01	0x01	0x00
	SMBus3	Speaker AMP L	0x10	0x01	0x01	0x00
		Speaker AMP R	0x10	0x01	0x01	0x00
		Thermal Monitor (G75311U)	0x10	0x01	0x01	0x00
		IR Thermal Sensor / MCU	0x10	0x01	0x01	0x00
	SMBus1	Accelerometer (BMA422)	0x10	0x01	0x01	0x00
		Accelerometer + Gyroscope (BMI160)	0x10	0x01	0x01	0x00
		Magnetometer (BMI150)	0x10	0x01	0x01	0x00
		Thermal Monitor (G781-1)	0x10	0x01	0x01	0x00
	SMBus2AUX	PD (TP56598CG)	0x10	0x01	0x01	0x00



TCP Port Signal Mapping for HDMI*

Description	Signal Mapping	
	TCP	HDMI
Main Link (Tx)	TCP_TX0	HDMI Data_2
	TCP_TX1	HDMI Data_0
	TCP_TXRX0	HDMI Data_1
	TCP_TXRX1	HDMI CLK

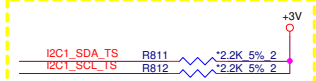
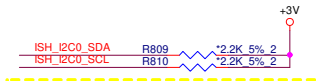
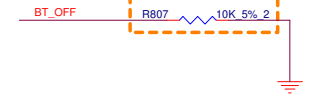
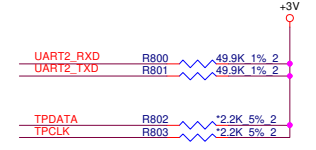
Note: Apply to TCP ports only.



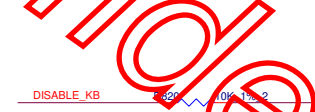
PROJECT : LVC
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Size Custom	Document Number ICL-U 1/14 (DDI/TBT/eDP)	Rev 3A
Date: Thursday, October 17, 2019	Sheet 4	of 91

CNVI_EN# PD 75K @ WLAN side
need Check with BIOS



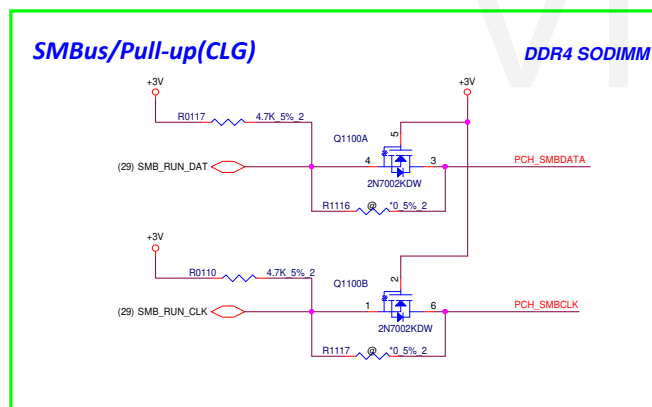
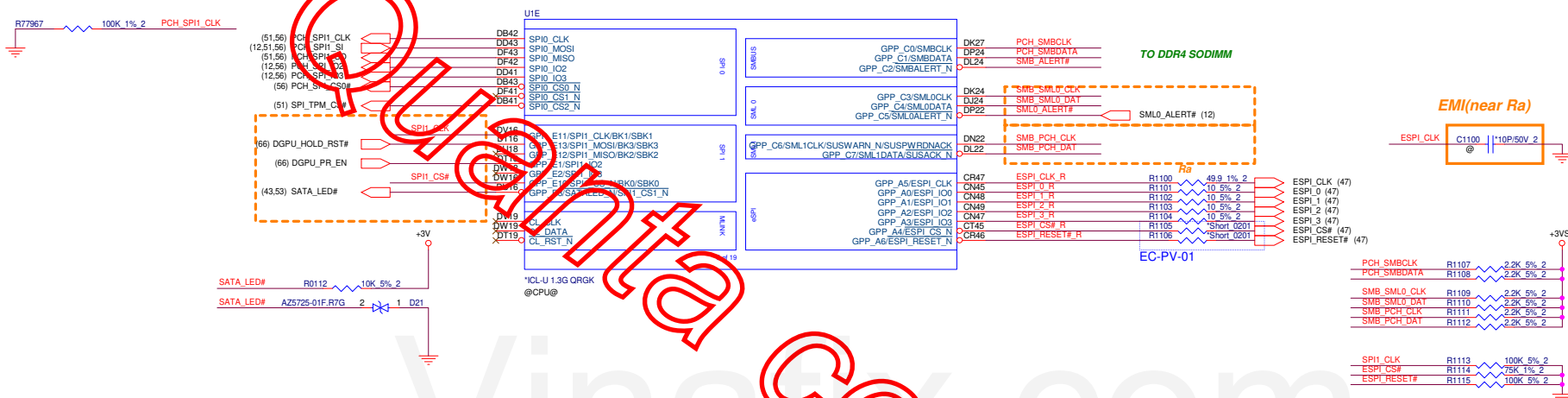
Correct Power rail to +3V
0610

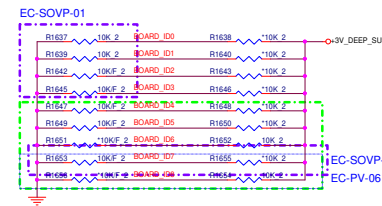
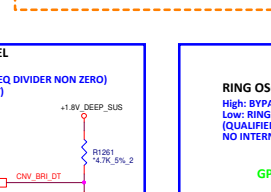
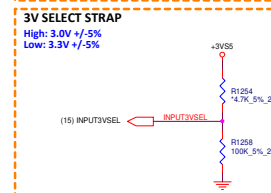
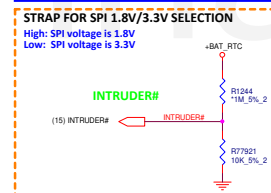
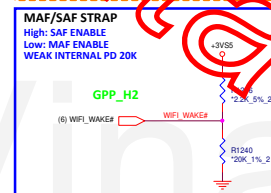
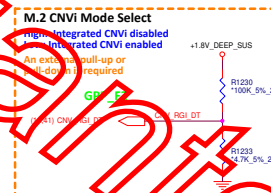
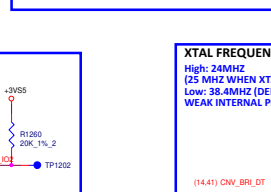
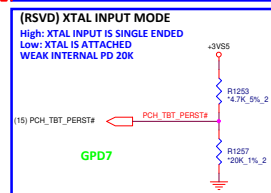
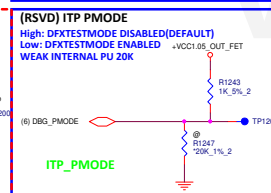
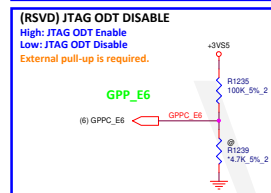
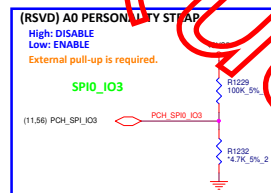
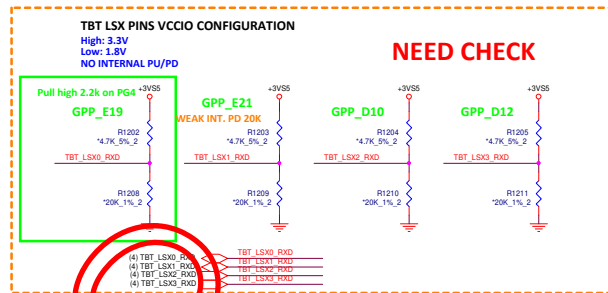
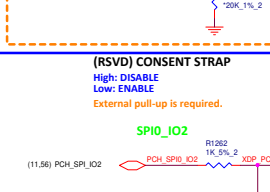
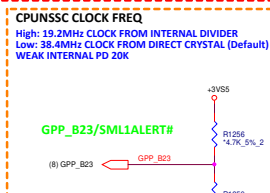
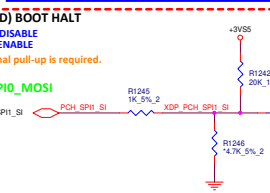
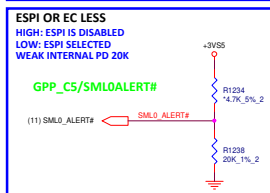
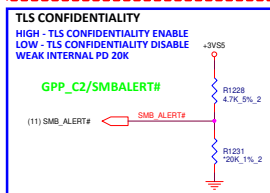
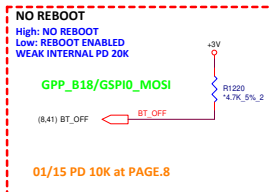
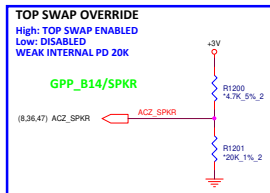


0617 remove LID circuit by Wayne

strap pin

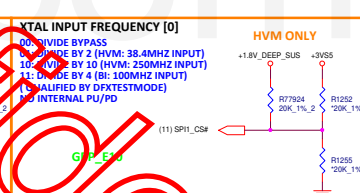
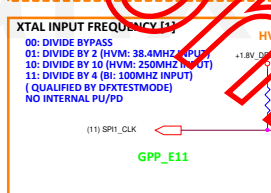
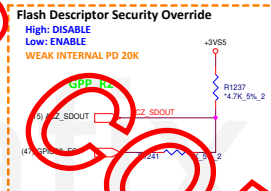






EC-SI-04

WHL-U	BOARD_ID8	BOARD_ID7	BOARD_ID6	BOARD_ID5	BOARD_ID4	BOARD_ID[3:0]				
Model	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
LVAC LVAD	EVT	0	0	13 inch	0	Software TPM	0	DIS	0	0
	FVT	0	1	14 inch	1	Hardware TPM	1	UMA	1	0
	SIT	1	0	15 inch	0					0
	MP	1	1	NA	1					0
										0
										0
										0
										0
										0
										0
										0
										0
										0
										0
										0
										0
										0







EC_VSTBY0
Slave Addresses:1000000

EC
Slave Addresses:1000001

EC
Slave Addresses:1000010

TBD
Slave Addresses:

CO-LAY WITH R4740

CO-LAY WITH L4700

CO-LAY WITH L4701

+VNN_EXT
Slave Addresses:1000100

TBD
Slave Addresses:

TBD
Slave Addresses:

+VCC1P8A
Slave Addresses:1000111

Placed close PR531

Placed close PR650

TBD
Slave Addresses:

TBD
Slave Addresses:

TBD
Slave Addresses:

TBD
Slave Addresses:

TBD
Slave Addresses:

TBD
Slave Addresses:

TBD
Slave Addresses:

TBD
Slave Addresses:

eDP
Slave Addresses:1001100

LCD Backlight
Slave Addresses:1000101

CO-LAY WITH L3402

CO-LAY WITH F3400

TBD
Slave Addresses:

Touch Screen Board sensor
Slave Addresses:1000011

CO-LAY WITH L3400

TBD
Slave Addresses:

TBD
Slave Addresses:

Codec
Slave Addresses:1000110

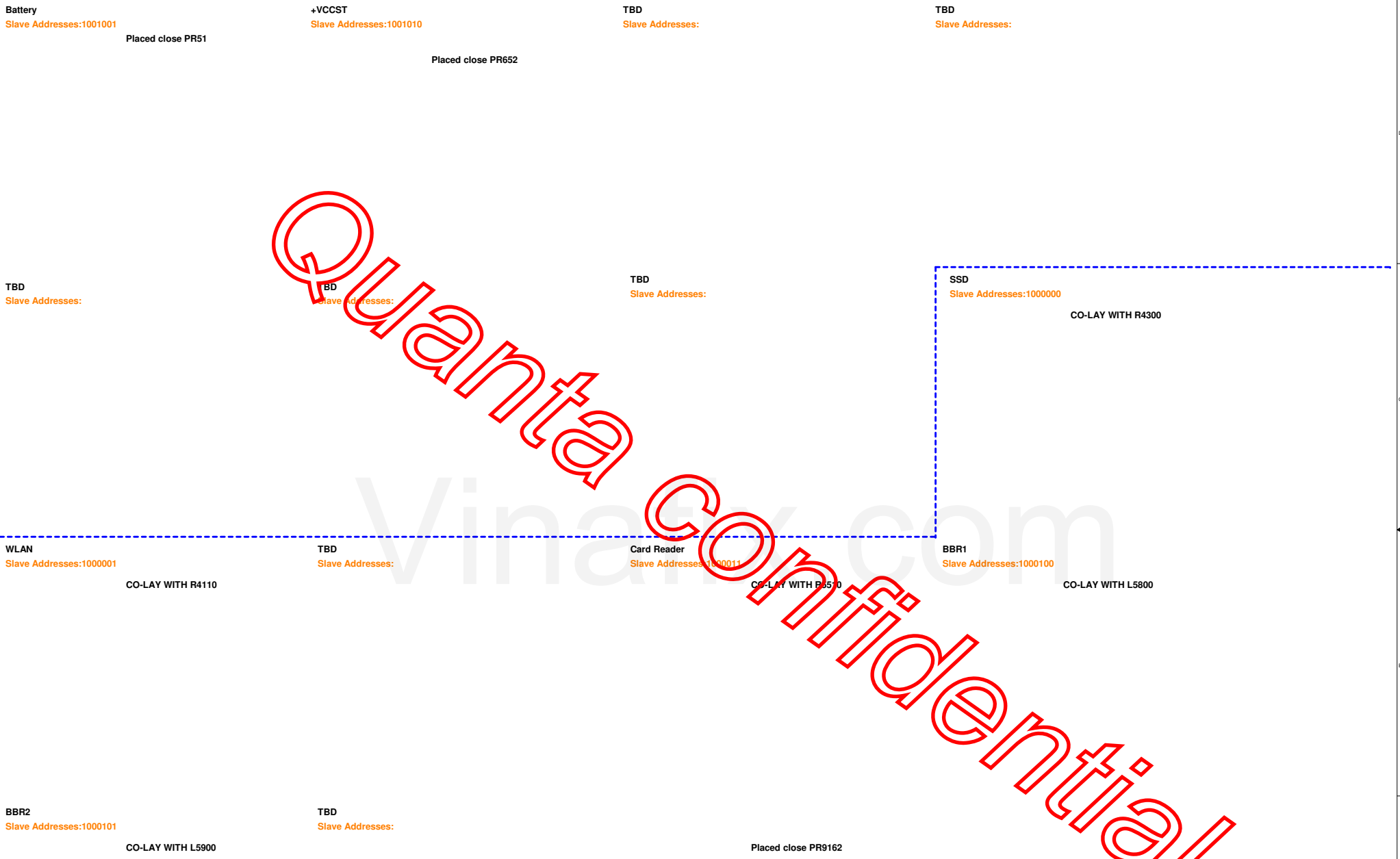
CO-LAY WITH L3602

USB-A
Slave Addresses:1001101

CO-LAY WITH R5735

WWAN
Slave Addresses:1001000

CO-LAY WITH R4217



Battery
Slave Addresses:1001001

+VCCST
Slave Addresses:1001010

TBD
Slave Addresses:

TBD
Slave Addresses:

TBD
Slave Addresses:

SSD
Slave Addresses:1000000

CO-LAY WITH R4300

WLAN
Slave Addresses:1000001

CO-LAY WITH R4110

TBD
Slave Addresses:

Card Reader
Slave Addresses:1000011

CO-LAY WITH R4500

BBR1
Slave Addresses:1000100

CO-LAY WITH L5800

BBR2
Slave Addresses:1000101

CO-LAY WITH L5900

TBD
Slave Addresses:

Placed close PR51

Placed close PR652

Placed close PR9162

+1.1VSUS
Slave Addresses:1001000

+0.6VSUS
Slave Addresses:1001001

+5V
Slave Addresses:1001010

TBD
Slave Addresses:

Placed close PR9195

TBD
Slave Addresses:

TBD
Slave Addresses:

TBD
Slave Addresses:

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Reserve

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Quanta Reserve

Vinamfx.com

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Reserve



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Reserve

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Reserve

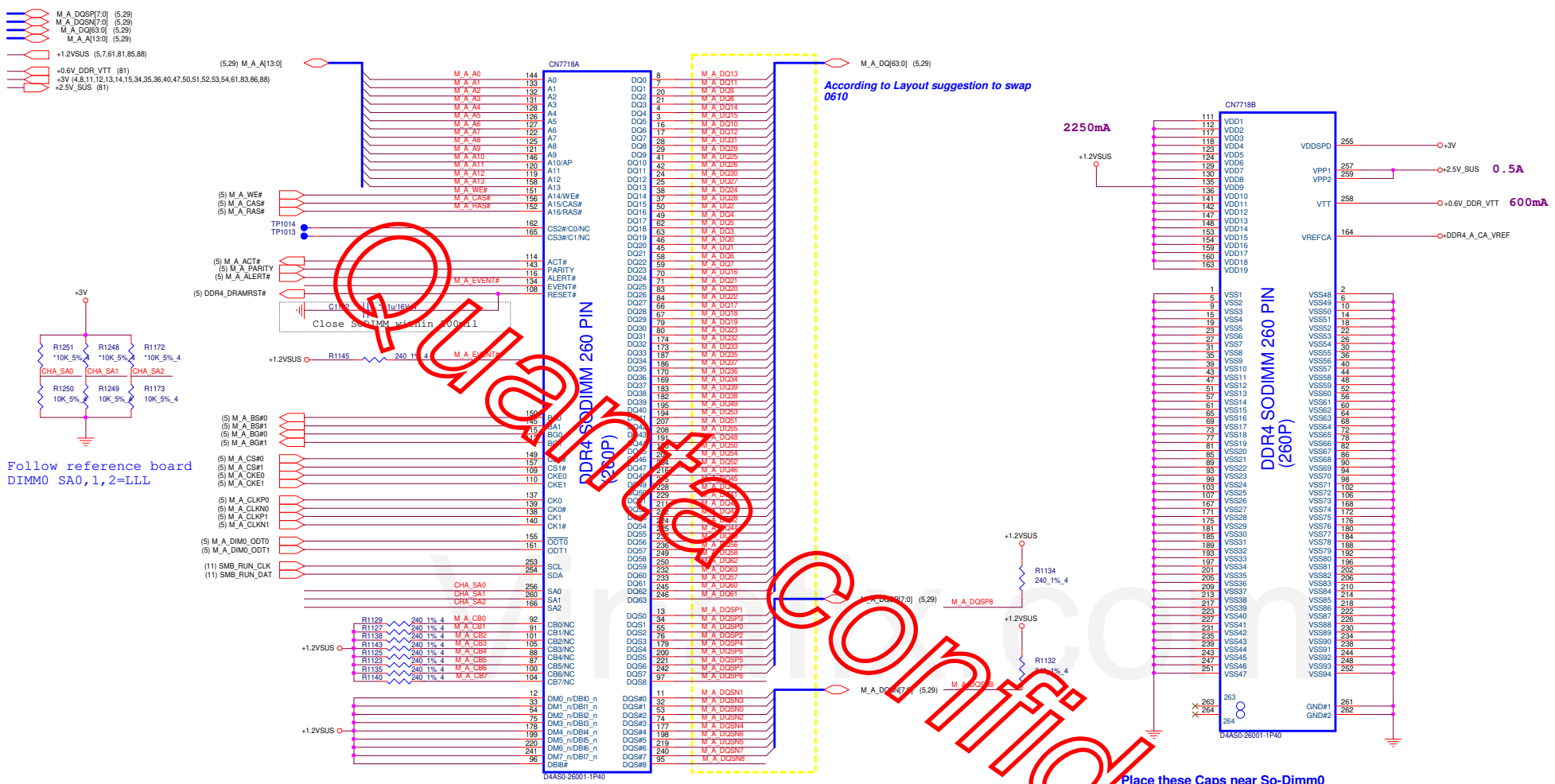
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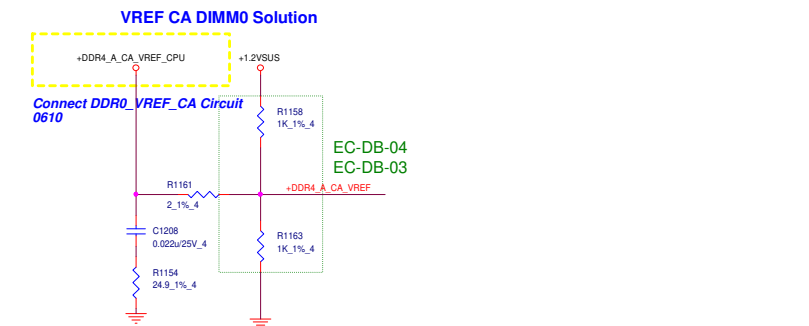
Signal	Value
M_A_DQS[7:0]	(5,29)
M_A_DQS[3:0]	(5,29)
M_A_Q[3:0]	(5,29)
M_A_Q[13:0]	(5,29)
+1.2V_SUS	(5,7,61,81,85,88)
+0.6V_DDR_VTT	(81)
+3V	(4,8,11,12,13,14,15,34,35,36,40,47,50,51,52,53,54,61,83,86,88)
+2.5V_SUS	(81)



Follow reference board
DIMM0 SA0,1,2=LL

According to Layout suggestion to swap 0610

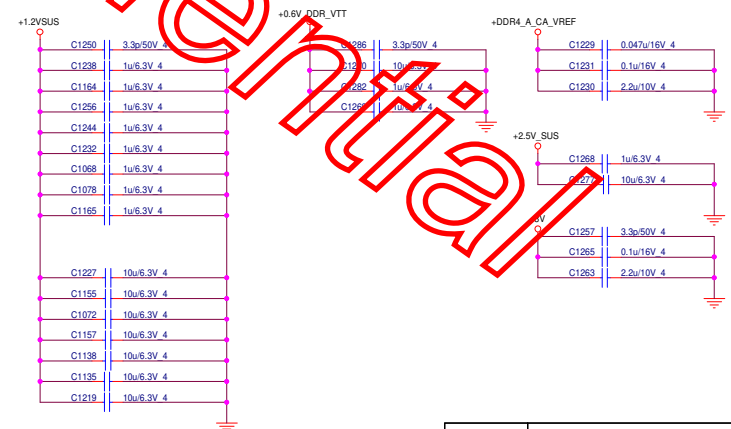
Place these Caps near So-Dimm0



Workaround

DDRO/1_VREF_CA pull up resistors to be changed to 200 ohms (instead of 1Kohm),
pull down resistors to be changed to 604 ohms (instead of 1Kohm).
Please see Figure 4-19 at ICL PDG doc # 572907 for reference.

- Workaround Impact - None



Remove by Wayne

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BU2			3A
Thursday, October 17, 2019		15:00:00	01

Remove by Wayne

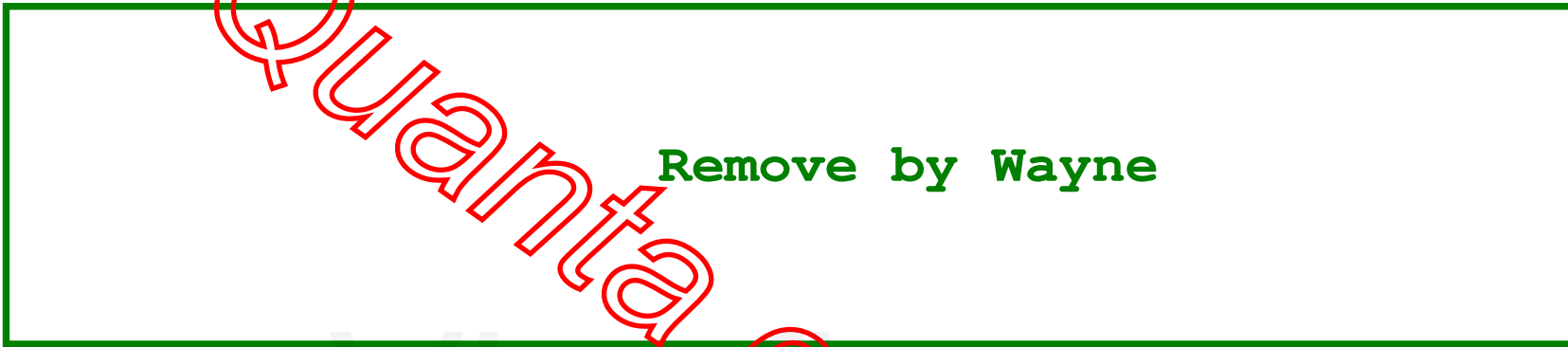
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Customer Doc#	Size	Document Number	Rev
BU2			3A
Thursday, October 17, 2019	10:04	Sheet	01



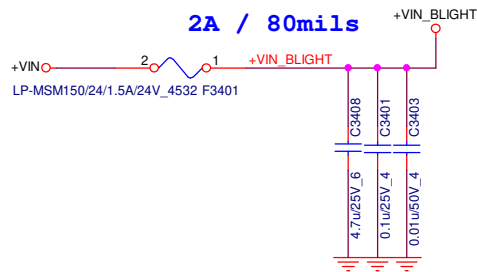
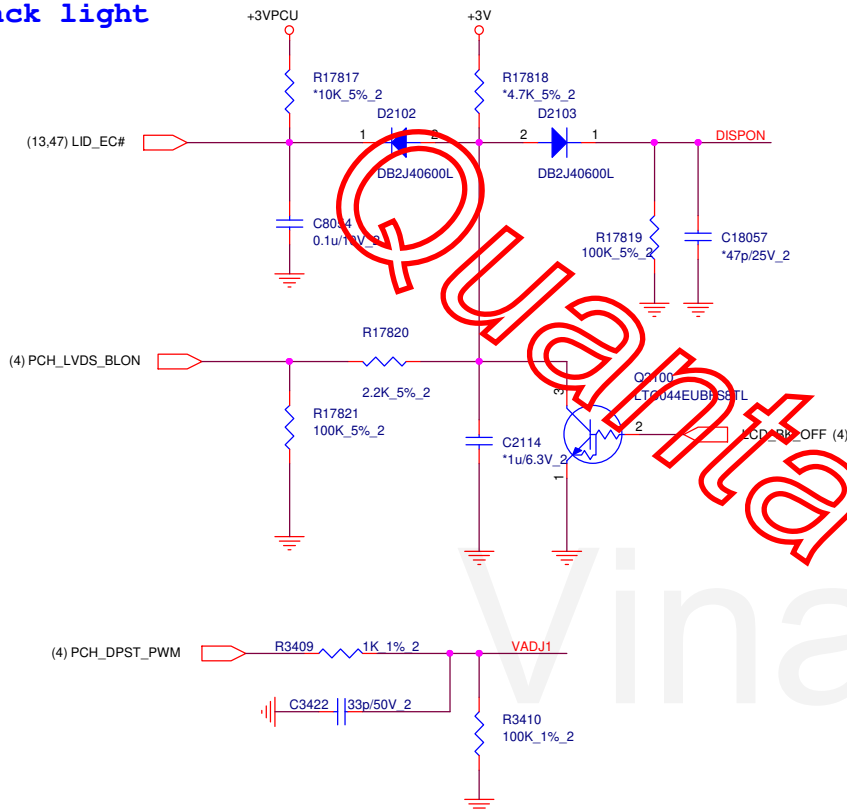


Reserve

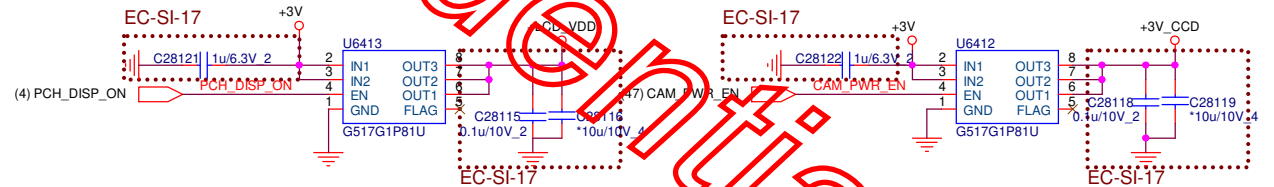
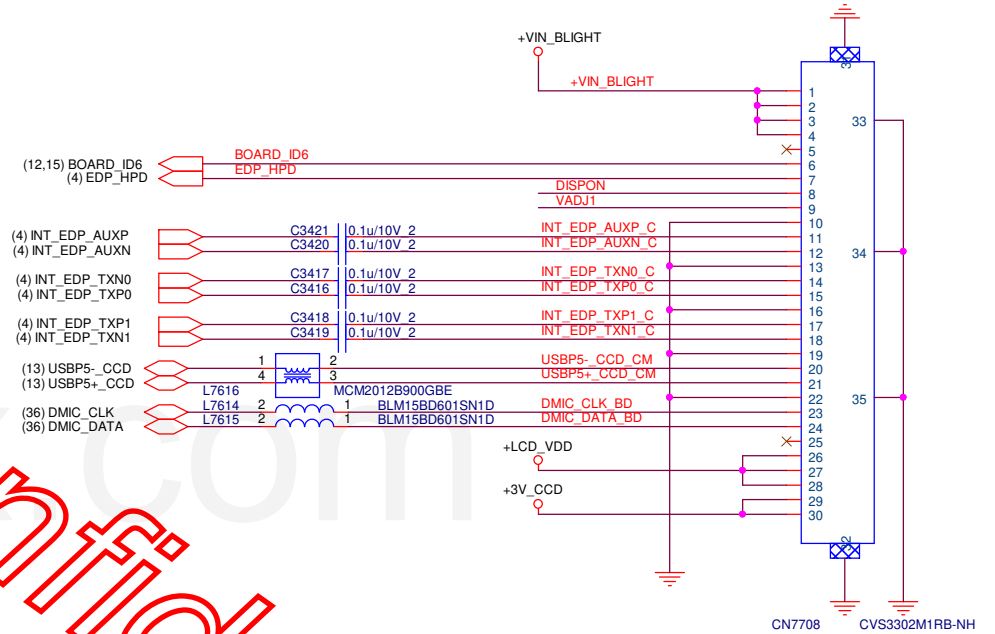
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Back light



eDP Connector



USBP5- CCD_CM	1	CH1	NC#1	10	USBP5- CCD_CM
USBP5+ CCD_CM	2	CH2	NC#2	9	USBP5+ CCD_CM
DMIC_CLK	3	GND#1	GND#2	8	DMIC_CLK
DMIC_DATA	4	CH3	NC#3	7	DMIC_DATA
	5	CH4	NC#4	6	DMIC_DATA

E5D U12 PUB3FR4

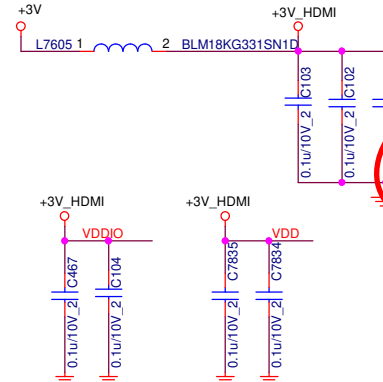


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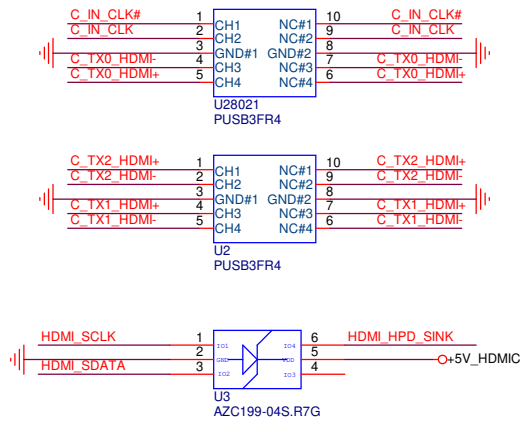
Size	Document Number	Rev
eDP/CAMMIC		3A

Thursday, October 17, 2019 1:50:00 PM

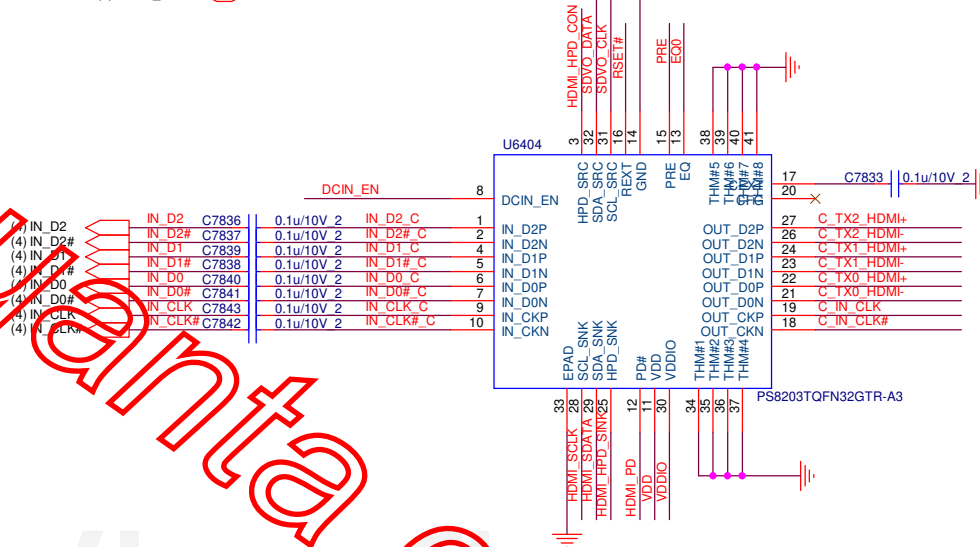
Close to Chip



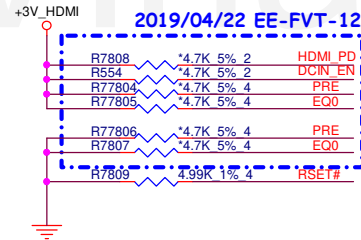
Close to HDMI connector



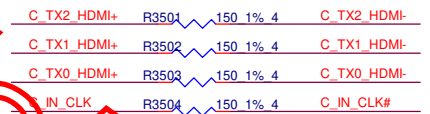
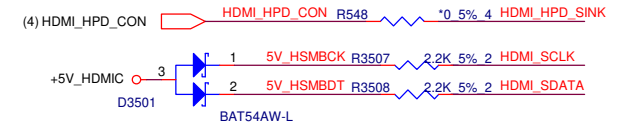
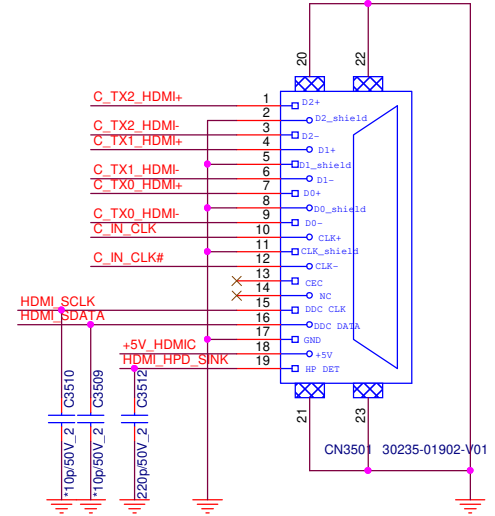
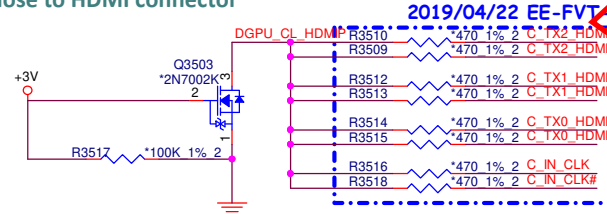
(4) SDVO_CLK
(4) SDVO_DATA



Internal Pull down 150K on HDMI_HPDI_SINK



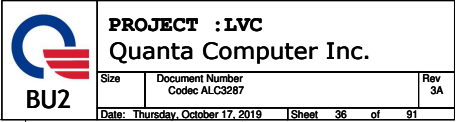
Close to HDMI connector



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Size	Document Number	Rev
	HDMI	3A
Date:	Thursday, October 17, 2019	Sheet 35 of 91

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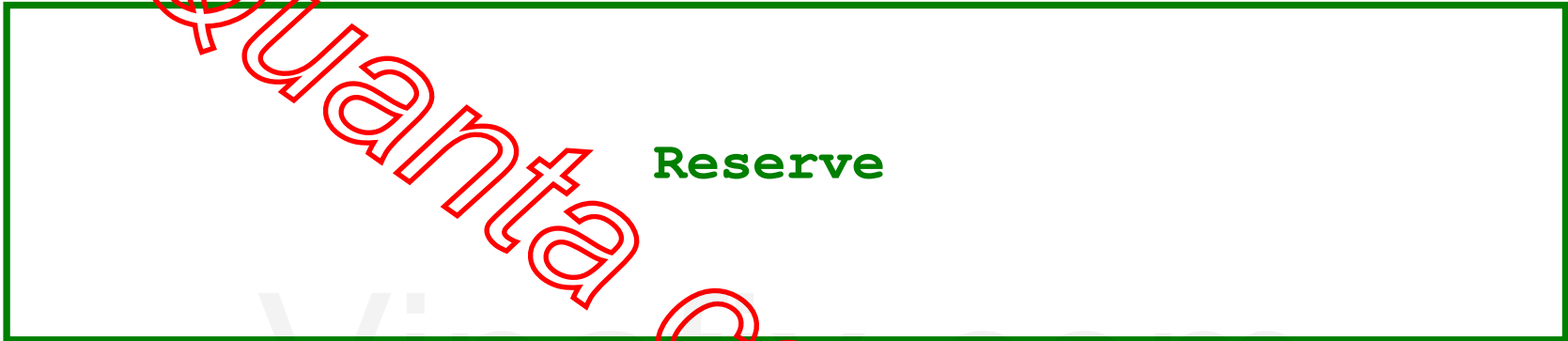


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 Customer BU2	PROJECT : LVC Quanta Computer Inc.		
	Size	Document Number	Rev
	Thursday, October 17, 2019	Audio Combo Jack	3A

AUDIO



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Customer Doc	Size	Document Number	Rev
BU2			3A
Thursday, October 17, 2019	15:06	01	

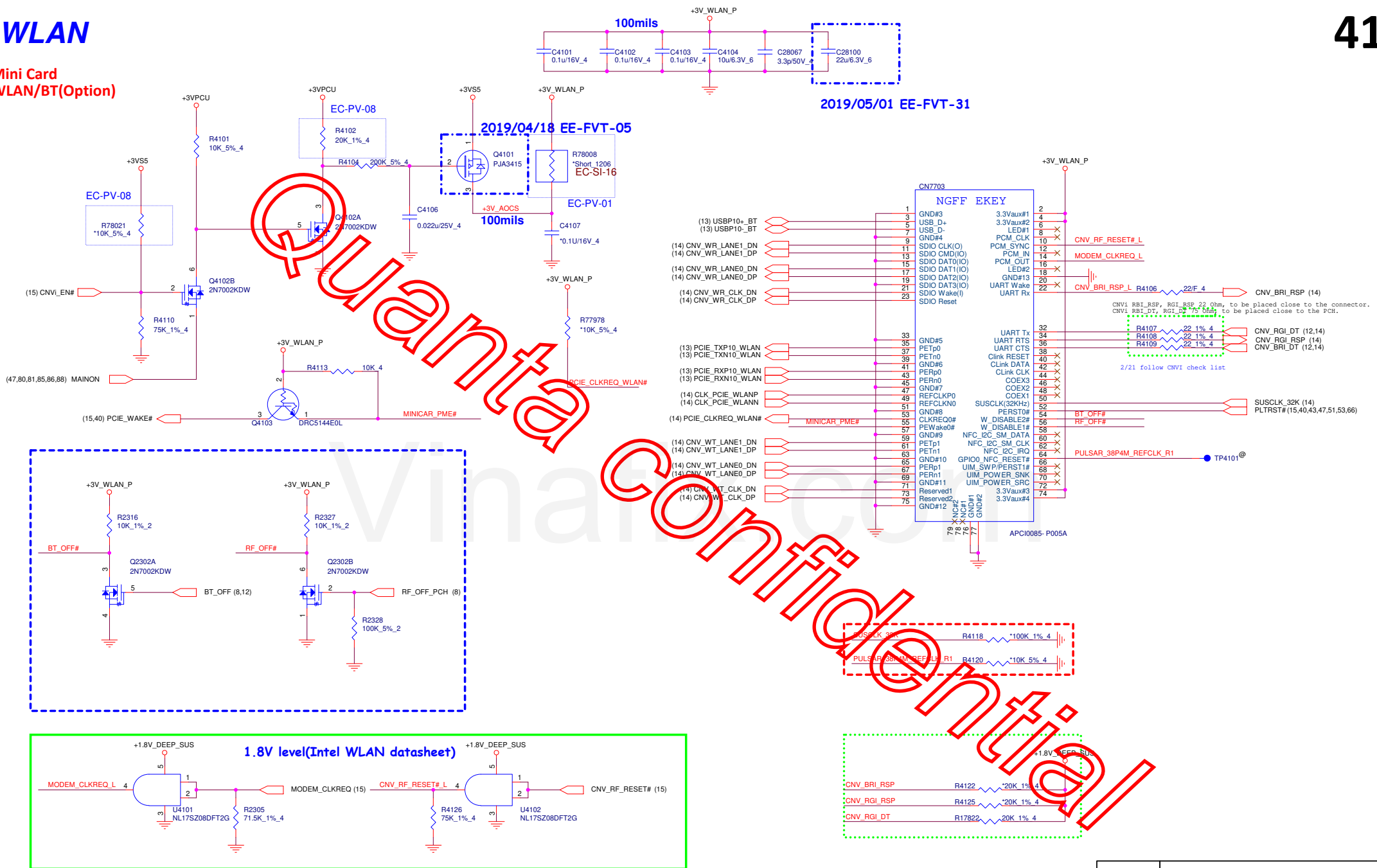


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**Mini Card
WLAN/BT(Optional)**

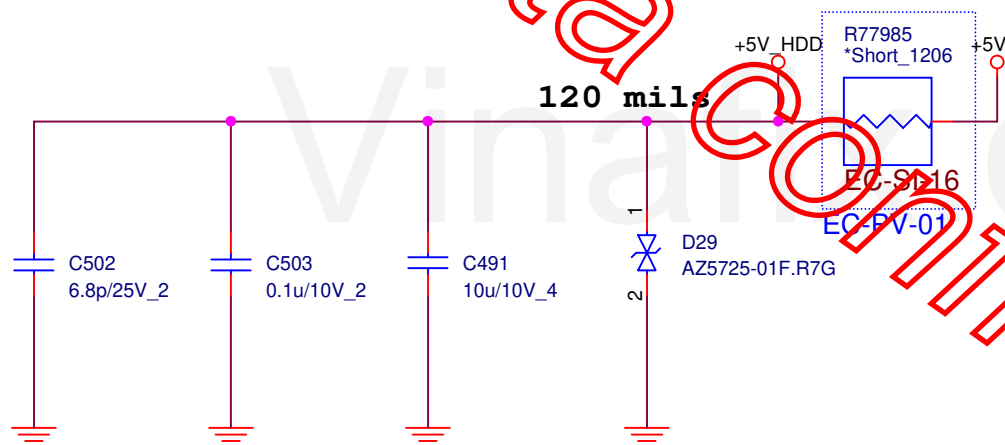
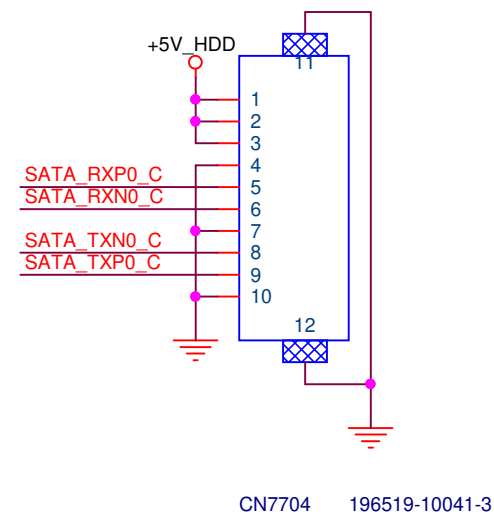
2019/05/01 EE-FVT-31





Reserve

(13) SATA1A_TXP	C137	0.01u/10V 2	SATA_TXP0_C
(13) SATA1A_TXN	C138	0.01u/10V 2	SATA_TXN0_C
(13) SATA1A_RXN	C139	0.01u/10V 2	SATA_RXN0_C
(13) SATA1A_RXP	C140	0.01u/10V 2	SATA_RXP0_C



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Size	Document Number	Rev
	2.5 Inch HDD	3A
Date:	Thursday, October 17, 2019	Sheet 44 of 91





Reserve

EC



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EC



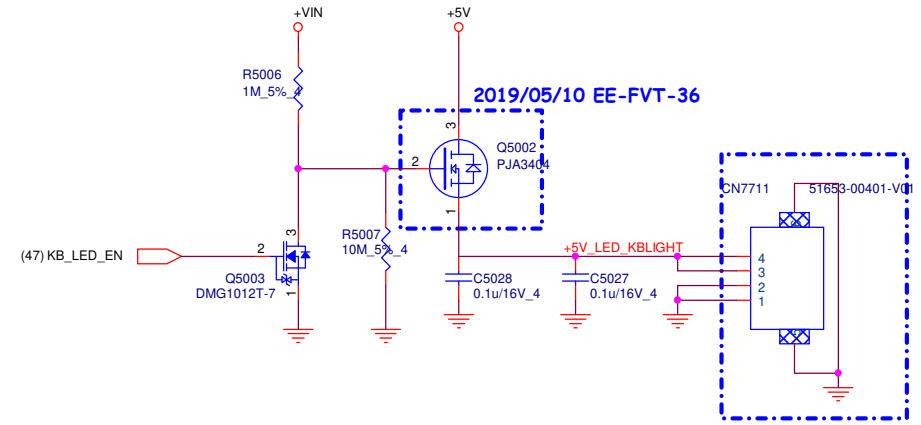
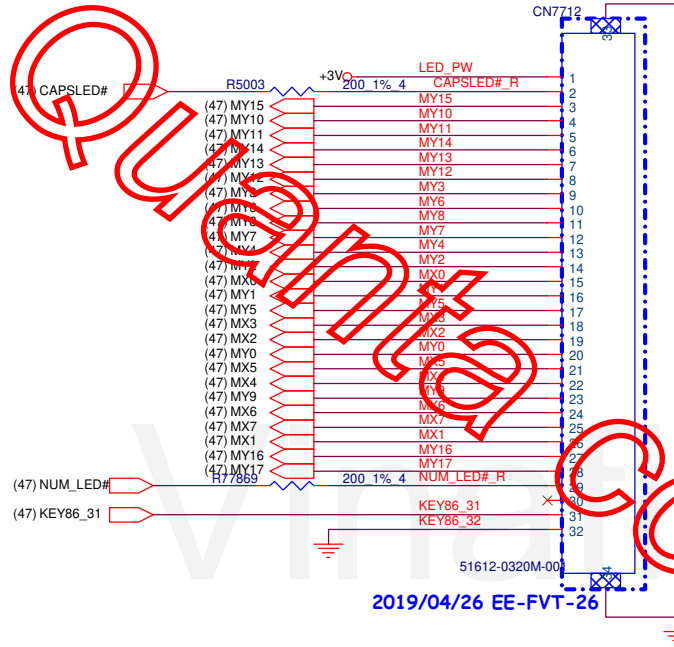
+3VS5 (4,5,10,11,12,15,16,40,41,47,52,57,61,65,66,73,76,78,80,81,82,84,85,86)
+3V (4,8,11,12,13,14,15,29,34,35,36,40,47,51,52,53,54,61,83,86,88)
+5VS5 (15,36,52,53,57,62,64,65,73,75,77,78,80,81,83,84,85,86)
+3VPCU (10,14,15,16,34,41,47,52,53,56,62,76,77,78,79,80,82,85,86)

KB LIGHT CONN (14")

50

KEYBOARD Con.

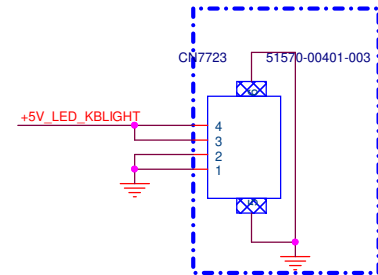
+3VPCUO R77870 10K 4 KEY86_31



KB LIGHT CONN (15")

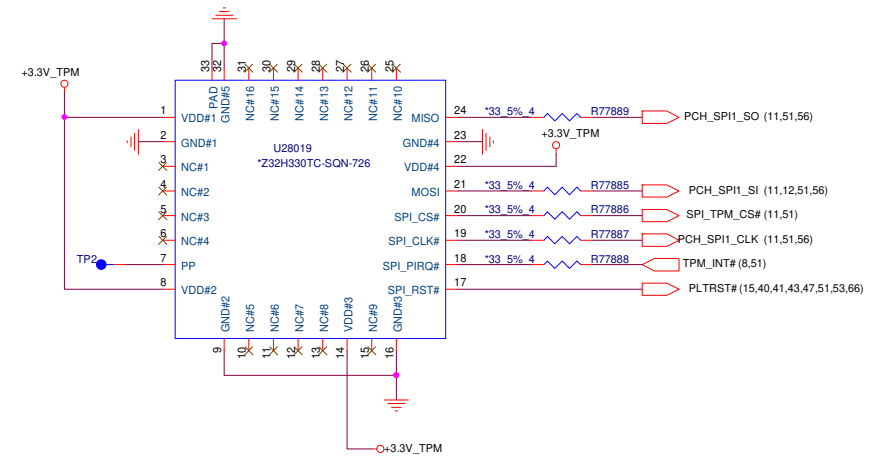
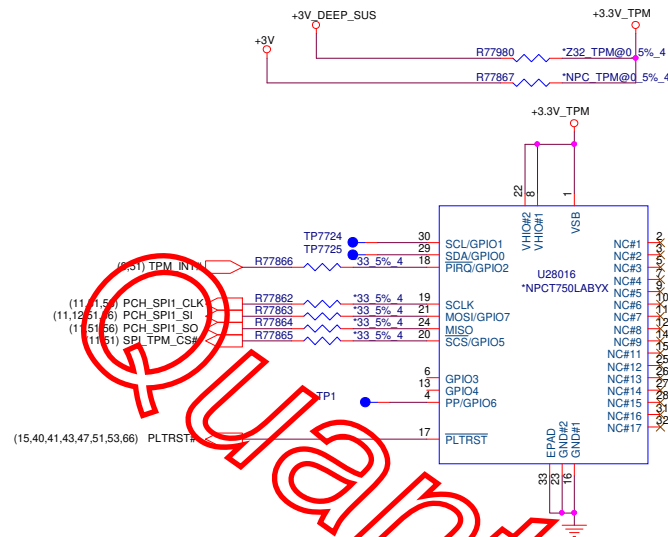
2019/05/01 EE-FVT-32

KEYBOARD PULL-UP		
MY0 C5011	220p/50V 2	
MY1 C5002	220p/50V 2	
MY2 C5005	220p/50V 2	
MY3 C5007	220p/50V 2	
MY4 C5008	220p/50V 2	
MY5 C5001	220p/50V 2	
MY6 C5004	220p/50V 2	
MY7 C5010	220p/50V 2	
MY8 C5013	220p/50V 2	
MY9 C5016	220p/50V 2	
MY10 C5019	220p/50V 2	
MY11 C5022	220p/50V 2	
MY12 C5015	220p/50V 2	
MY13 C5018	220p/50V 2	
MY14 C5021	220p/50V 2	
MY15 C5024	220p/50V 2	
MY16 C5025	220p/50V 2	
MY17 C5026	220p/50V 2	
MX0 C5006	220p/50V 2	
MX1 C5012	220p/50V 2	
MX2 C5023	220p/50V 2	
MX3 C5020	220p/50V 2	
MX4 C5014	220p/50V 2	
MX5 C5009	220p/50V 2	
MX6 C5017	220p/50V 2	
MX7 C5003	220p/50V 2	



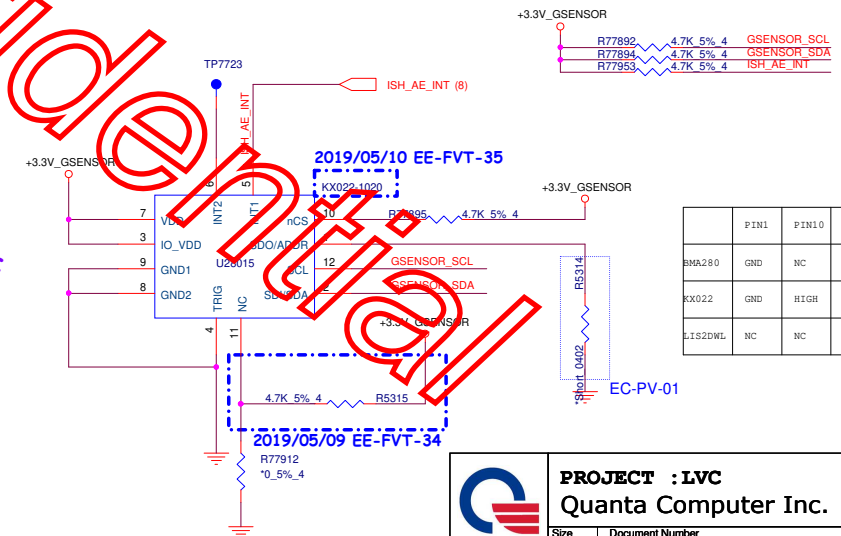
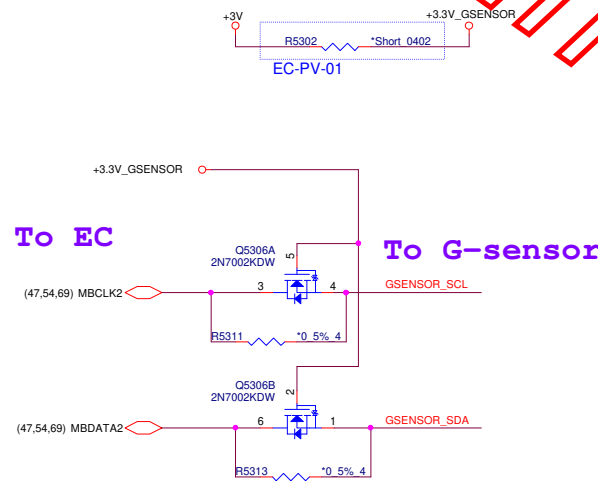
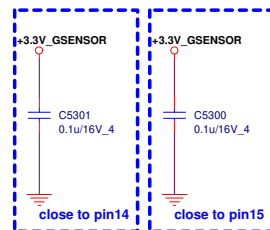
PROJECT : LVC
Quanta Computer Inc.

Size	Document Number	Rev
	Keyboard/Keyboard Backlight	3A
Date: Thursday, October 17, 2019	Sheet 50 of 91	



Order Number ¹	Package ²	Temperature	TPM 2.0 Library Revision	FW Version
NPCT750xAAYX	QFN32	Standard	01.16	7.2.0.1
NPCT758xAAYX	UQFN16	Standard	01.16	7.2.0.1
NPCT754xAAYX	QFN32	Wide	01.16	7.2.0.1
NPCT75CxAYX	UQFN16	Wide	01.16	7.2.0.1
NPCT750xABYX	QFN32	Standard	01.38	7.2.1.0
NPCT758xABYX	UQFN16	Standard	01.38	7.2.1.0
NPCT754xABYX	QFN32	Wide	01.38	7.2.1.0
NPCT75CxABYX	UQFN16	Wide	01.38	7.2.1.0

G Sensor



	PIN1	PIN10	PIN11
BMA280	GND	NC	HIGH
KX022	GND	HIGH	NC
LIS2DWL	NC	NC	NC



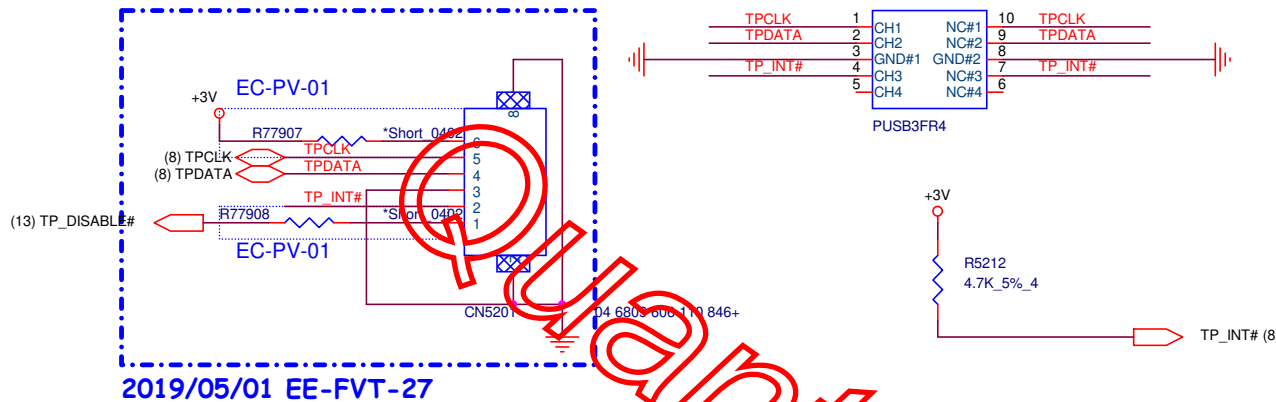
PROJECT : LVC
Quanta Computer Inc.

Size	Document Number	Discrete TPM	Rev
3A			

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Touch Pad

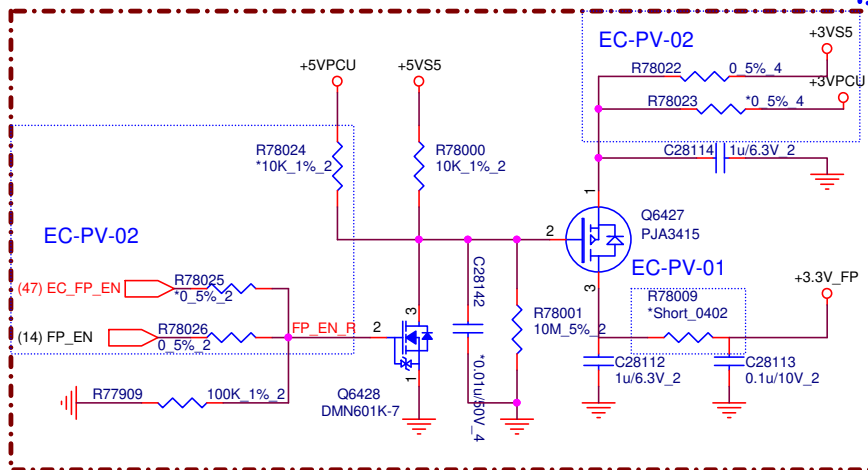
52



Finger print

2019/04/26 EE-FVT-23

EC-SI-07



2019/04/25 EE-FVT-20

Pin No.	Symbol	Description
1	LED	LED SIGNAL
2	RESETN	MCU RESETN SIGNAL
3	GPIO_AL0	POWER SHIELD
4	DELINK	POWER STATUS
5	DGND	GROUND
6	DP	USB DATA+
7	DM	USB DATA-
8	D3V3	POWER 3.3V

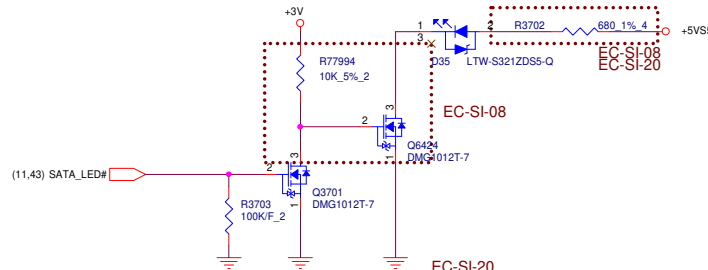
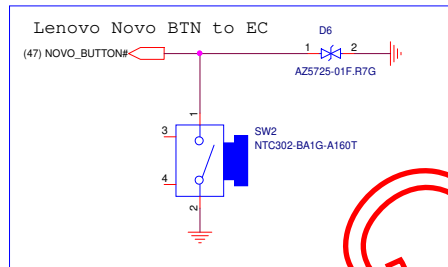


PROJECT : IVC
Quanta Computer Inc.

Size	Document Number	Rev
	Touch Pad/Fingerprint	3A
Date: Sunday, October 27, 2019	Sheet 52 of 91	

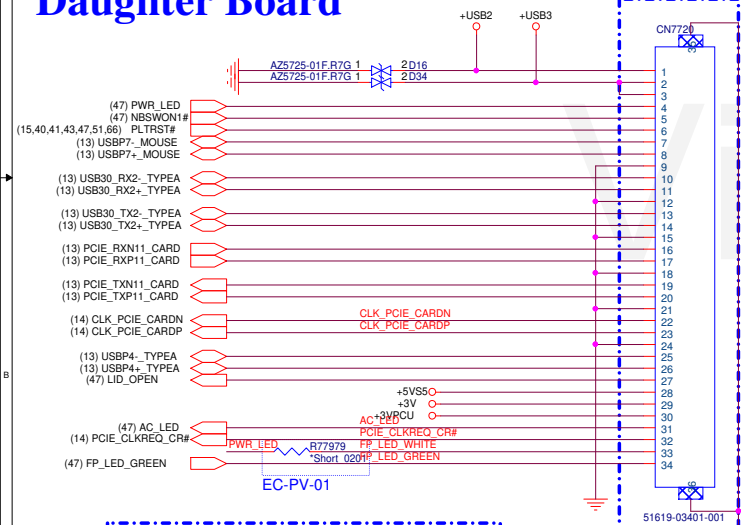
BU2

SENSOR



53

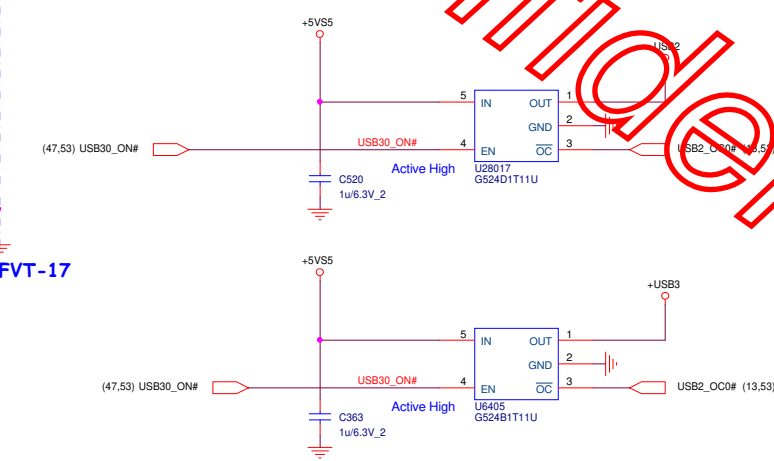
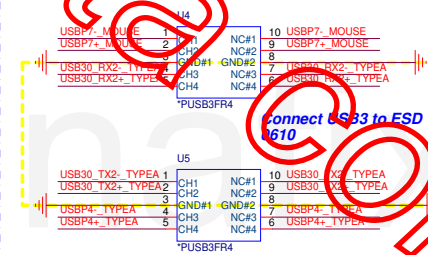
Daughter Board



2019/04/25 EE-FVT-18

2019/04/25 EE-FVT-17

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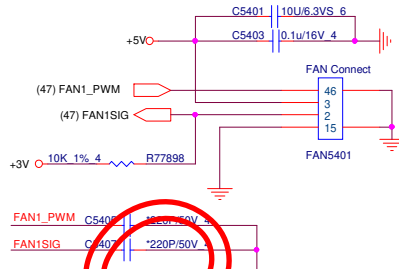


PROJECT :LVC
Quanta Computer Inc.

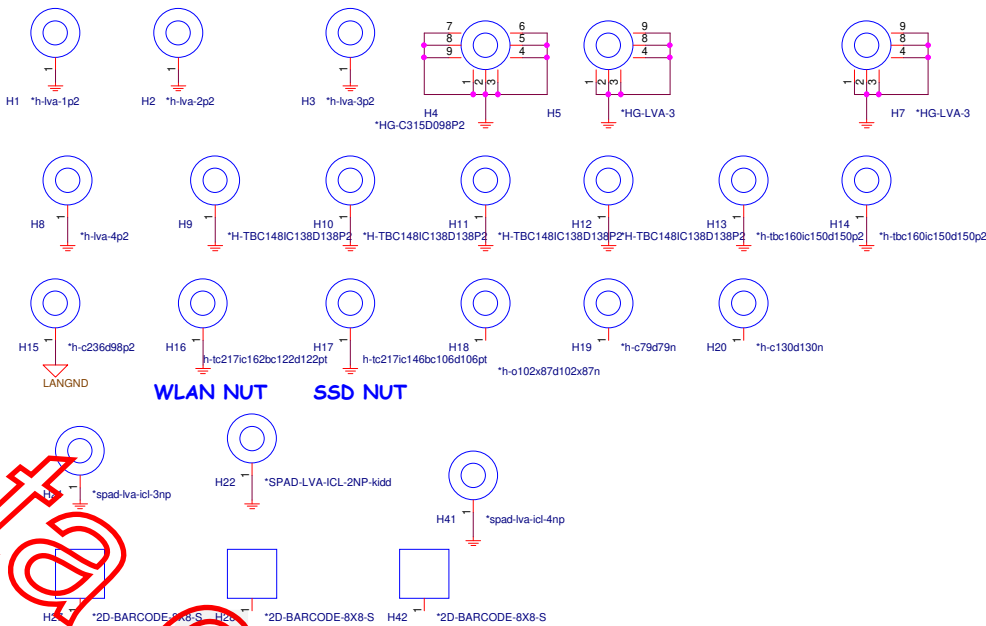
Size	Document Number	Rev
BU2		3A
Date:	Thursday, October 17, 2019	Sheet 53 of 91

FAN/Thermal

FAN



Hole

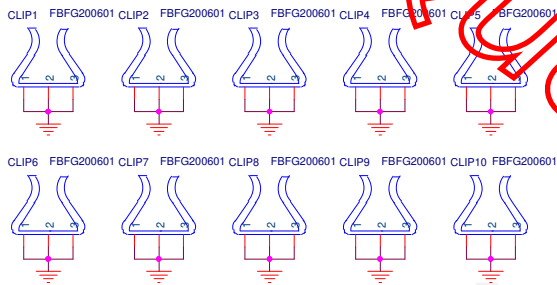


RF SPAD

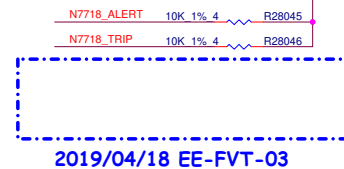
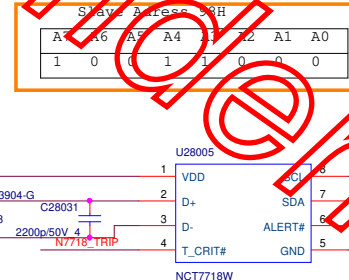
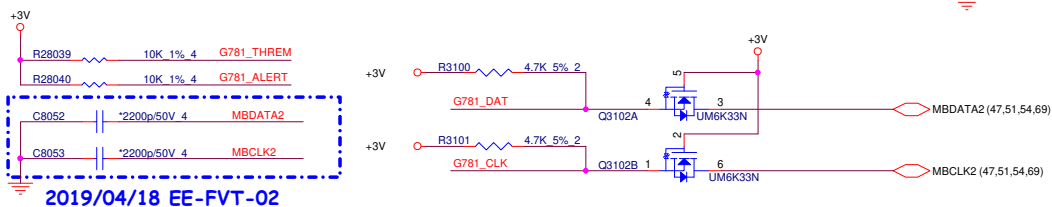
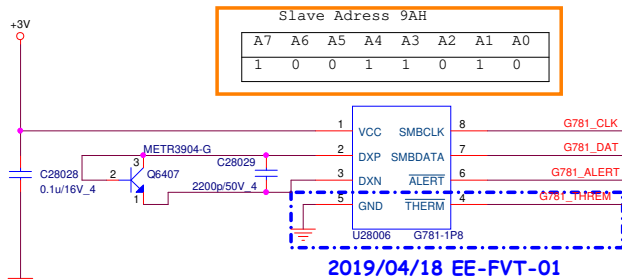
54



CLIP



Thermal Sensor



Nuvoton	NCT7718W	SMBus Address	98h	AL0007718001
Nuvoton	W83L771AWG-2	SMBus Address	9Ah	AL83L771K03
GMT	G781P8	SMBus Address	98h	AL000781012
GMT	G781-1P8	SMBus Address	9Ah	AL000781039



PROJECT : LVC		
Quanta Computer Inc.		
Size	Document Number	Rev
	FAN/Thermal Sensor	3A
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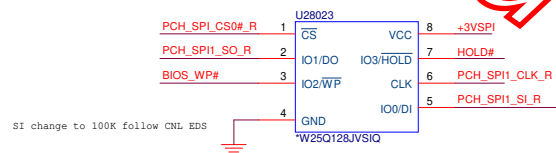
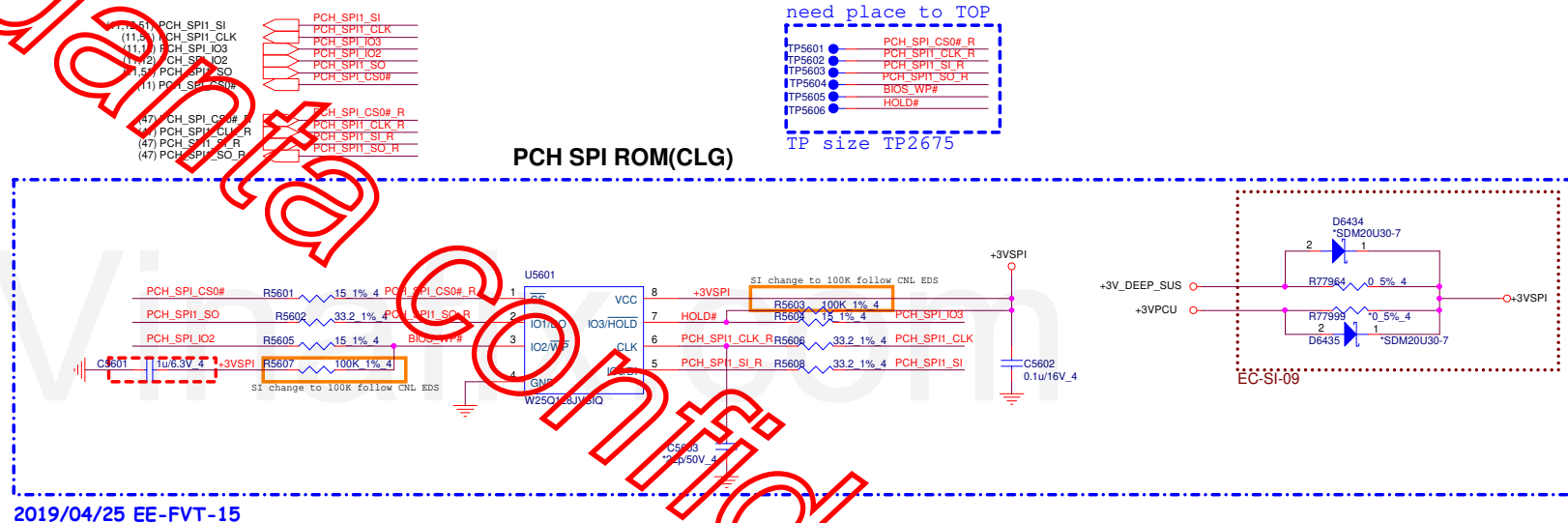
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FLASH ROM

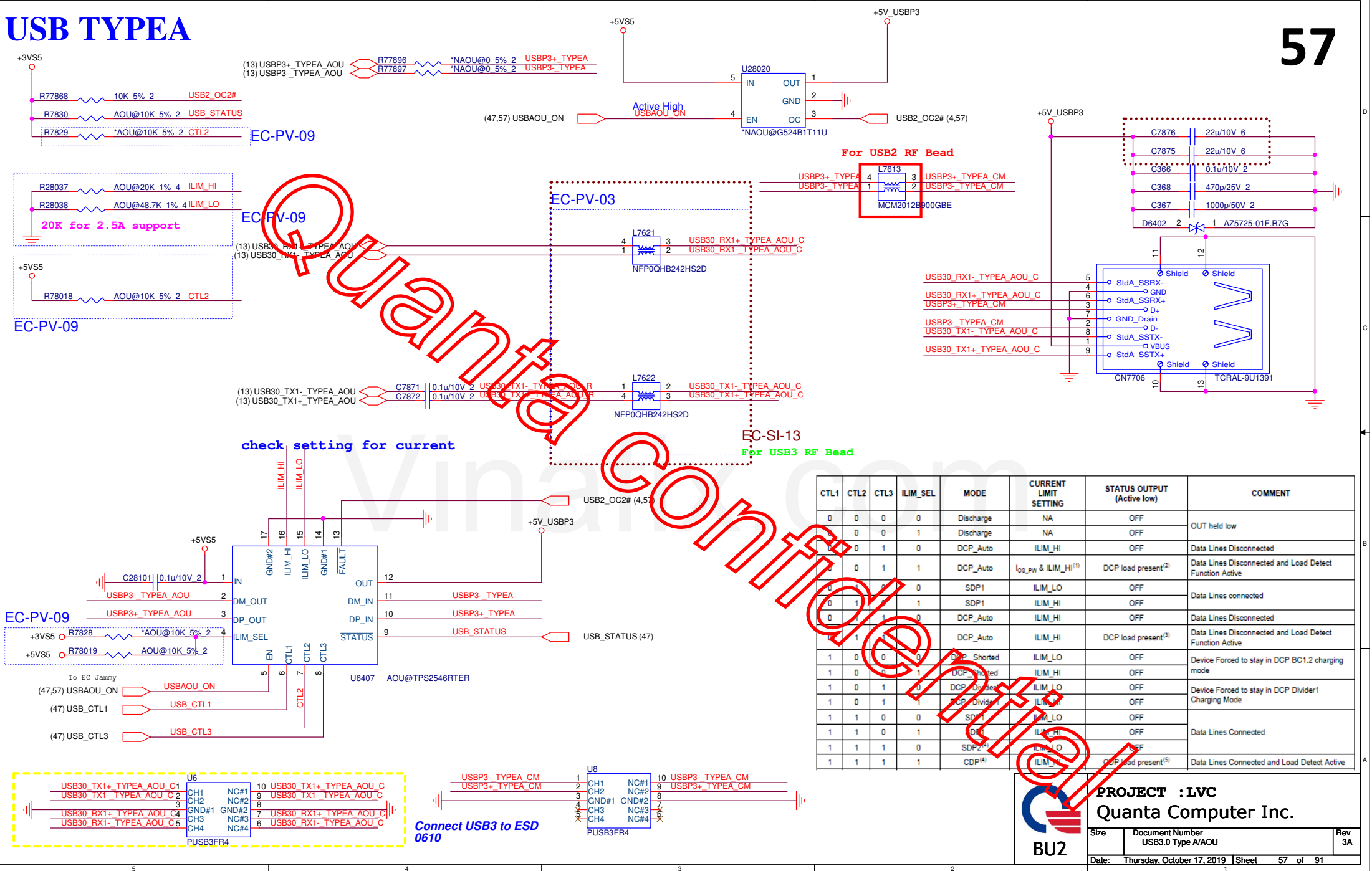
PCH SPI ROM

Vender	Size	P/N
MXIC	16MB	AKE3DZN0Z08(MX25L12872FM2L-10G)
Winbond	16MB	AKE3DF-KN01(W25Q128JVS1Q)
	16MB	
Socket		DG008000011




USB TYPEA

57



CTL1	CTL2	CTL3	ILIM_SEL	MODE	CURRENT LIMIT SETTING	STATUS OUTPUT (Active low)	COMMENT
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	OUT held low
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	0	1	1	DCP_Auto	loc_fw & ILIM_HI ⁽¹⁾	DCP load present ⁽²⁾	Data Lines Disconnected and Load Detect Function Active
0	1	0	0	SDP1	ILIM_LO	OFF	Data Lines connected
0	1	1	0	SDP1	ILIM_HI	OFF	Data Lines connected
0	1	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
1	0	1	0	DCP_Auto	ILIM_HI	DCP load present ⁽³⁾	Data Lines Disconnected and Load Detect Function Active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device Forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	Device Forced to stay in DCP BC1.2 charging mode
1	0	1	0	DCP_Divider	ILIM_LO	OFF	Device Forced to stay in DCP Divider1 Charging Mode
1	0	1	1	DCP_Divider	ILIM_HI	OFF	Device Forced to stay in DCP Divider1 Charging Mode
1	1	0	0	SDP1	ILIM_LO	OFF	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	OFF	Data Lines Connected
1	1	1	0	SDP2	ILIM_LO	OFF	Data Lines Connected
1	1	1	1	SDP2	ILIM_HI	DCP load present ⁽⁵⁾	Data Lines Connected and Load Detect Active

**PROJECT :LVC**
Quanta Computer Inc.

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BU2	USB3.0 Type A/AOU	3A
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Remove by Wayne

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Remove by Wayne

Quanta Confidential

Vinafix.com

Remove by Wayne

Quanta Confidential

Vinaia.com

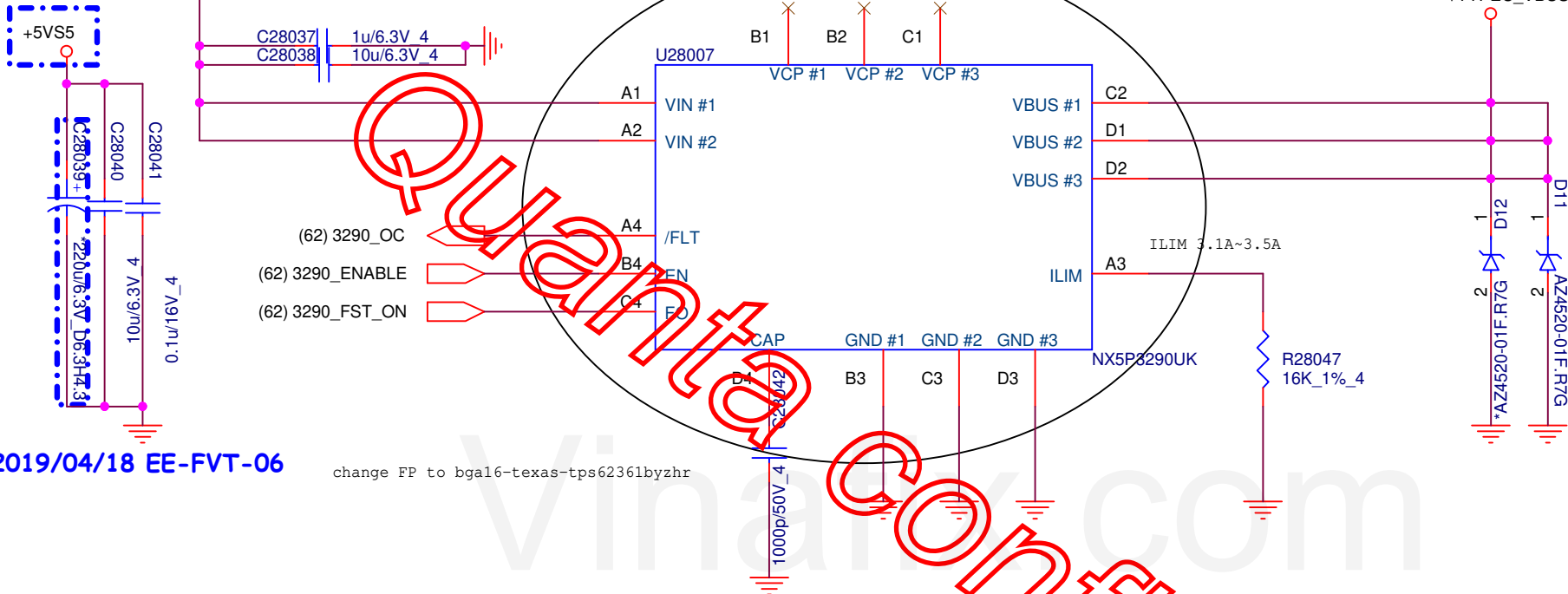


Remove by Wayne

TYPE-C Load Switch

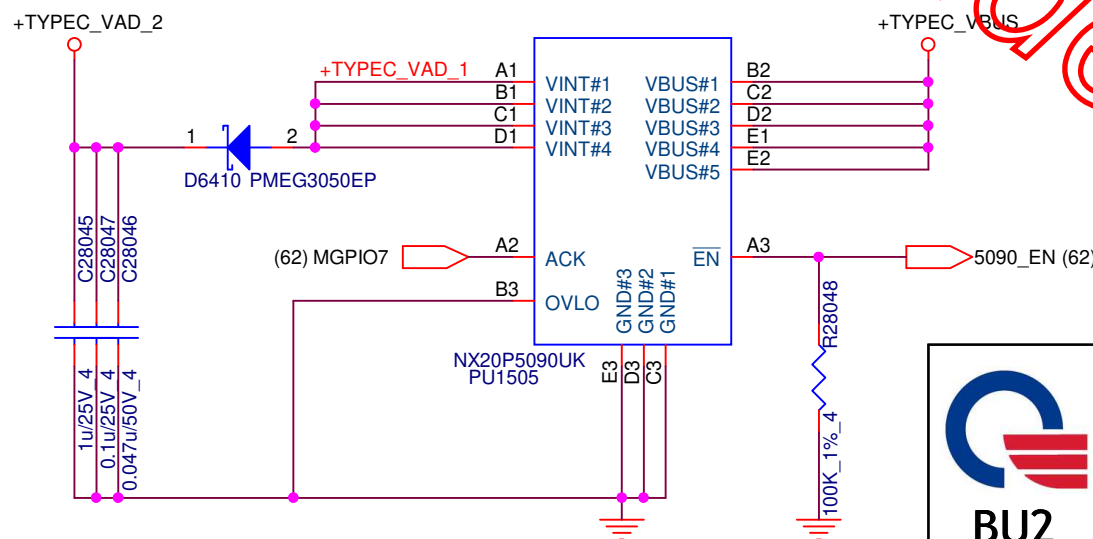
64

2019/04/22 EE-FVT-08



2019/04/18 EE-FVT-06

change FP to bga16-texas-tps62361byzhr

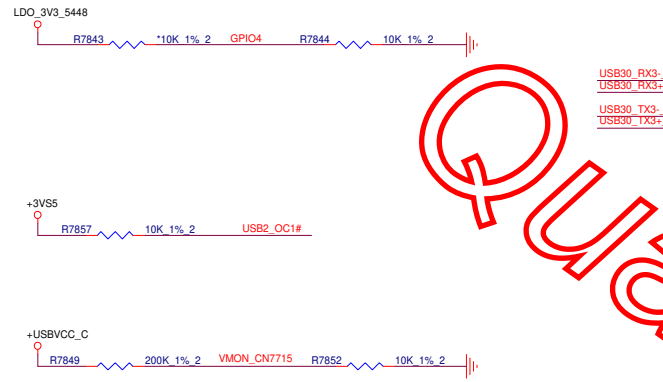


PROJECT : LVC
Quanta Computer Inc.

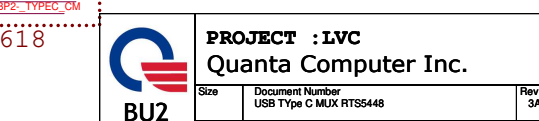
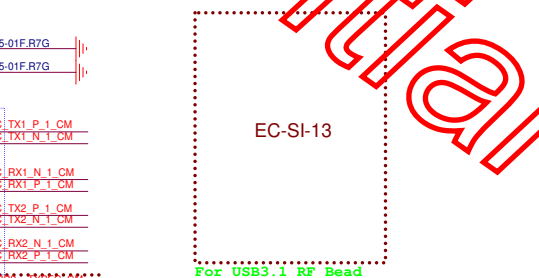
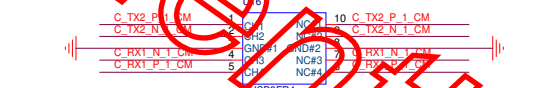
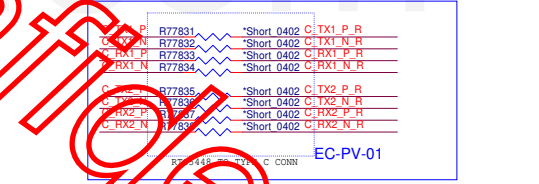
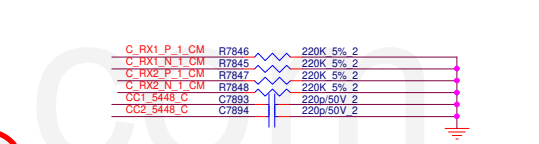
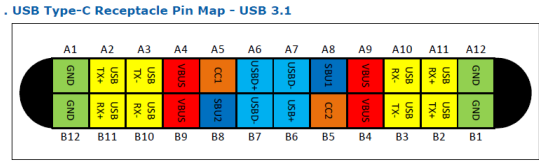
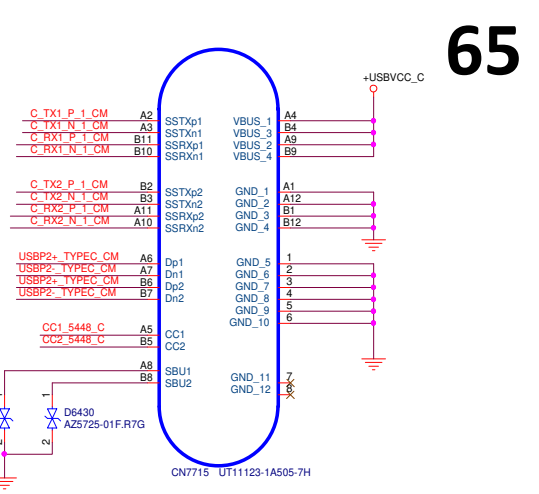
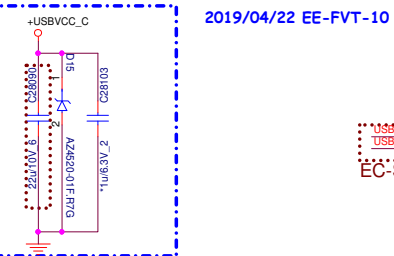
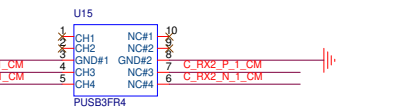
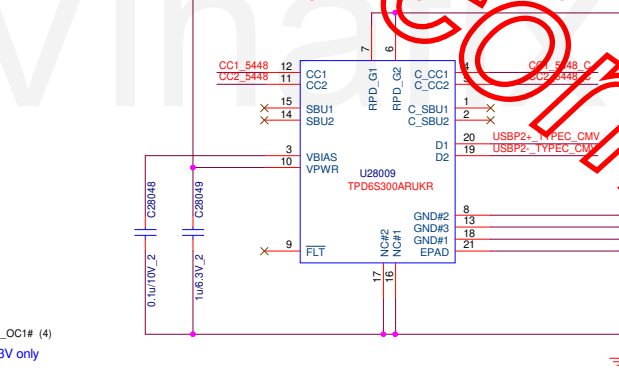
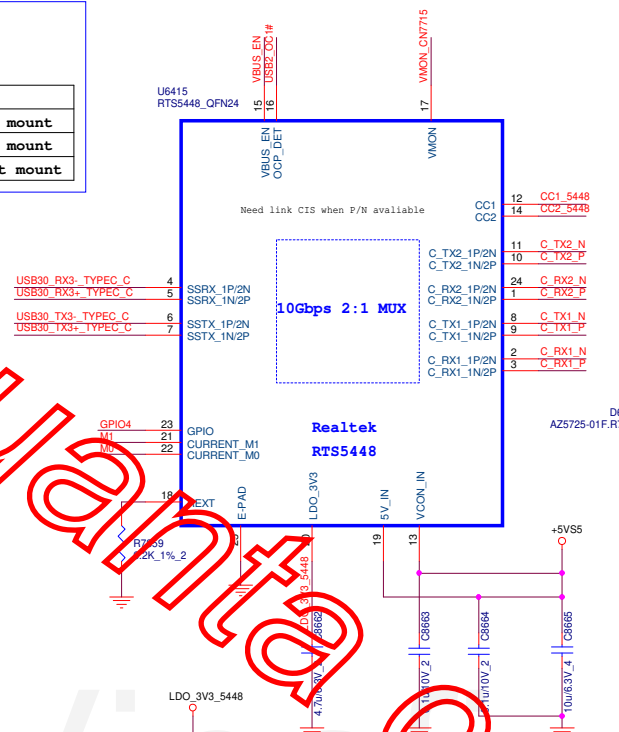
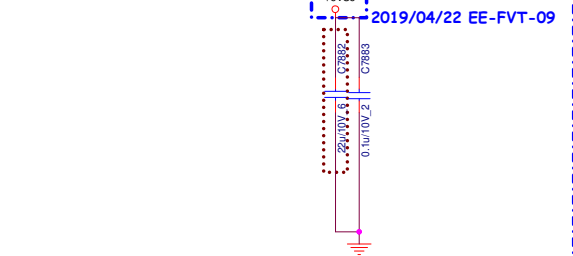
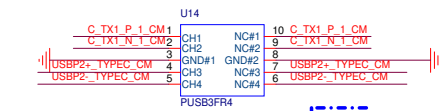
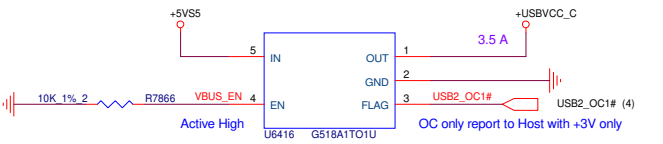
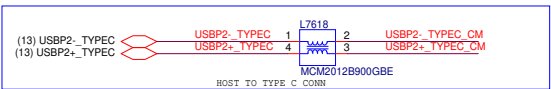
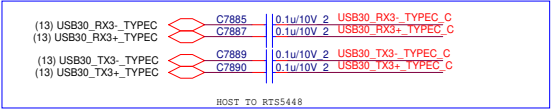
Size	Document Number	Rev
	Load Switch for Power Delivery	3A
Date: Thursday, October 17, 2019	Sheet 64 of 91	

Rp: 3A (now)

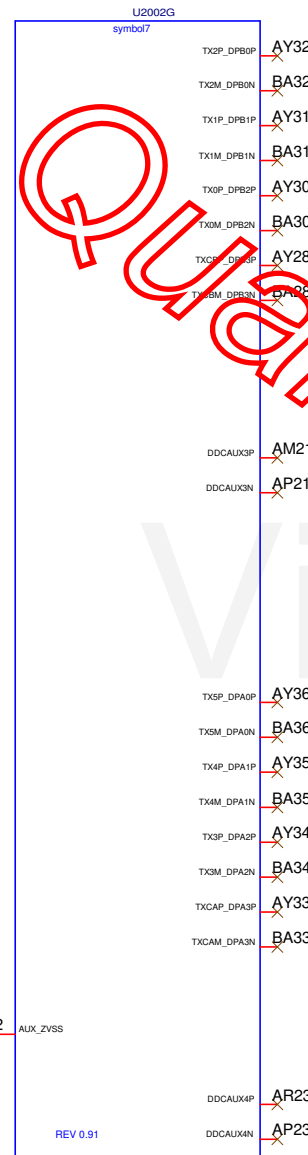
	M1	M0	Note
Rp: 900mA	0	1	R7851/R7853mount, R7850/R7854 don't mount
Rp: 1.5A	1	0	R7850/R7854mount, R7851/R7853 don't mount
Rp: 3.0A	1	1	R7850/R7851 mount, R7853/R7854 don't mount



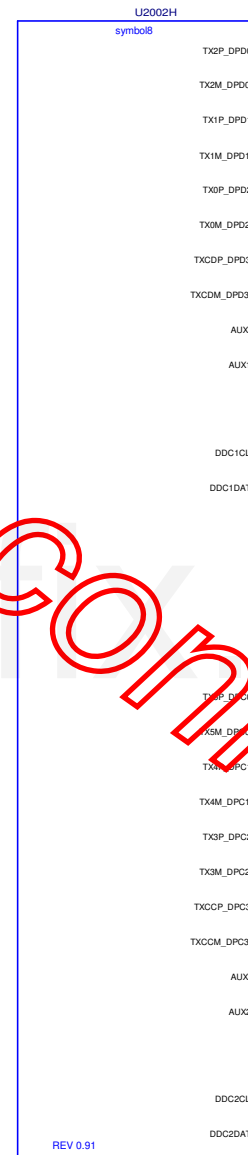
C.TX1_P_R	C7888	0.1u/10V_2	C.TX1_P_1	C.TX2_P_R	C7880	0.1u/10V_2	C.TX2_P_1
C.TX1_N_R	C7886	0.1u/10V_2	C.TX1_N_1	C.TX2_N_R	C7879	0.1u/10V_2	C.TX2_N_1
C.RX1_P_R	C7892	0.33u/25V_2	C.RX1_P_1	C.RX2_P_R	C7881	0.33u/25V_2	C.RX2_P_1
C.RX1_N_R	C7891	0.33u/25V_2	C.RX1_N_1	C.RX2_N_R	C7884	0.33u/25V_2	C.RX2_N_1



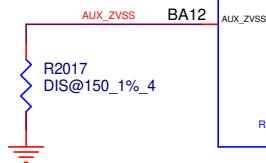
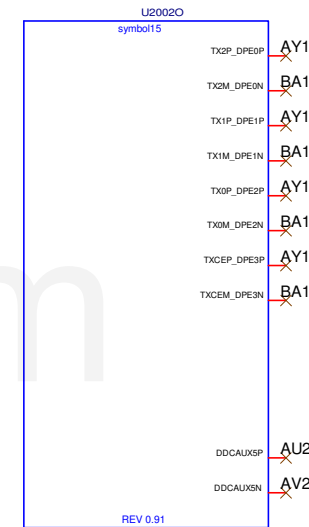
ASIC - TMDP (A/B)

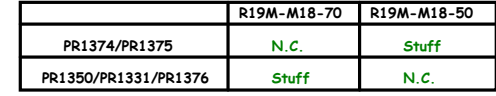


ASIC - TMDP (C/D)



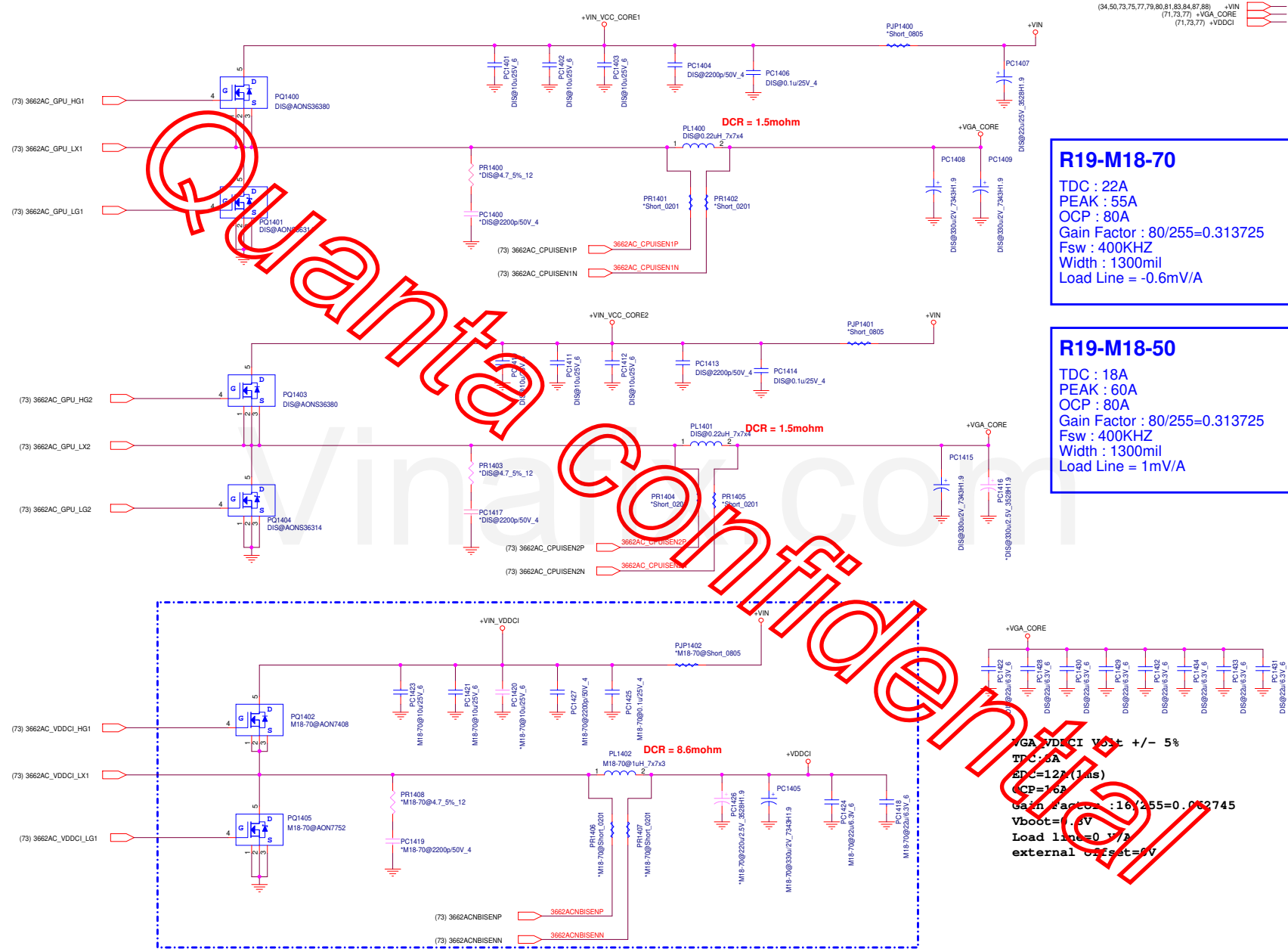
ASIC - TMDP (E)





	R19M-M18-70 LL=0.6m	R19M-M18-50 LL=1m
PR1356	Stuff 63.4k	NC
PR1379	NC	Stuff 38.3k

dGPU



PROJECT : IVC
Quanta Computer Inc.

Size C	Document Number	Rev 3A
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Vout=1.5V Ton R= 127K
Vout=1.35V Ton R= 113K

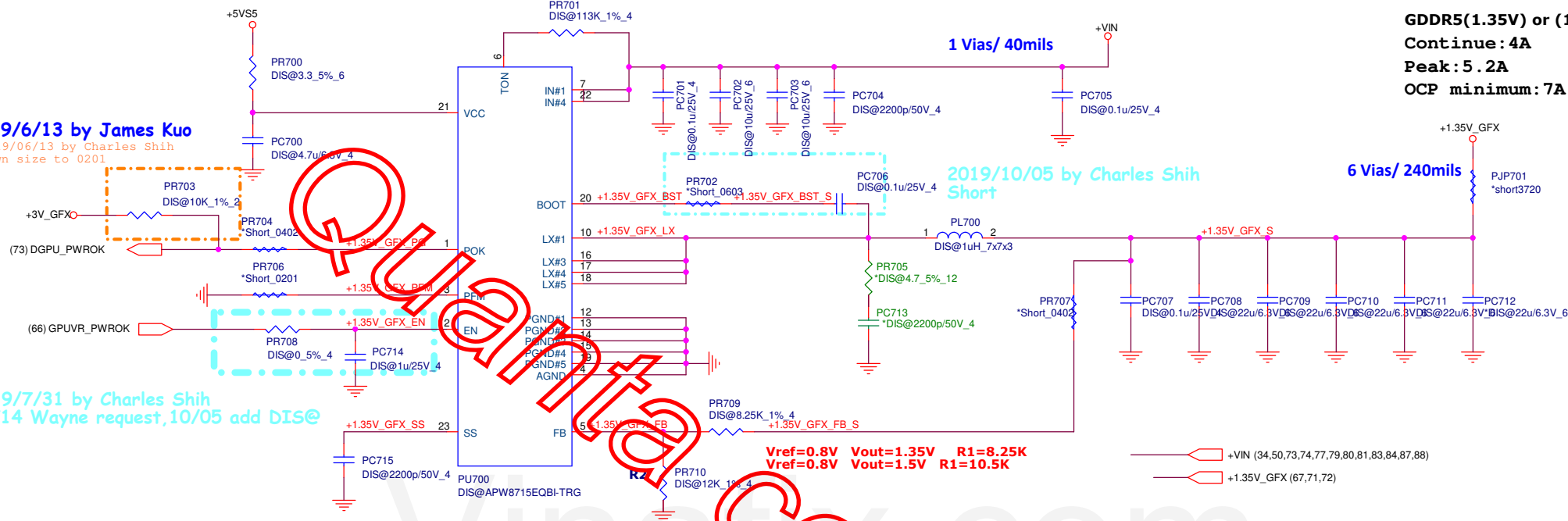
GDDR5(1.35V) or (1.5V)
Continue: 4A
Peak: 5.2A
OCP minimum: 7A

2019/6/13 by James Kuo

2019/06/13 by Charles Shih
Down size to 0201

2019/10/05 by Charles Shih
Short

2019/7/31 by Charles Shih
PC714 Wayne request, 10/05 add DIS@



PROJECT : LVC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.35V_VGA (APW8715)	3A
Date: Thursday, October 17, 2019	Sheet 75 of 91	

2019/05/09 by James Kuo
Per EE check result change to +3VPCU from +3VS5

(66,69,75) +3V_GFX
(66,69,70,71,73) +1.8V_GFX
(15,36,52,53,57,62,64,65,73,75,78,80,81,83,84,85,86) +5VS5
(34,50,73,74,75,79,80,81,83,84,87,88) +VIN
(4,5,10,11,12,15,16,40,41,47,52,57,61,65,66,73,76,78,80,81,82,84,85,86) +3VS5
(10,14,15,16,34,41,47,50,52,53,56,62,76,78,79,80,82,85,86) +3VPCU

2019/7/31 by Charles Shih
PC750 Wayne request

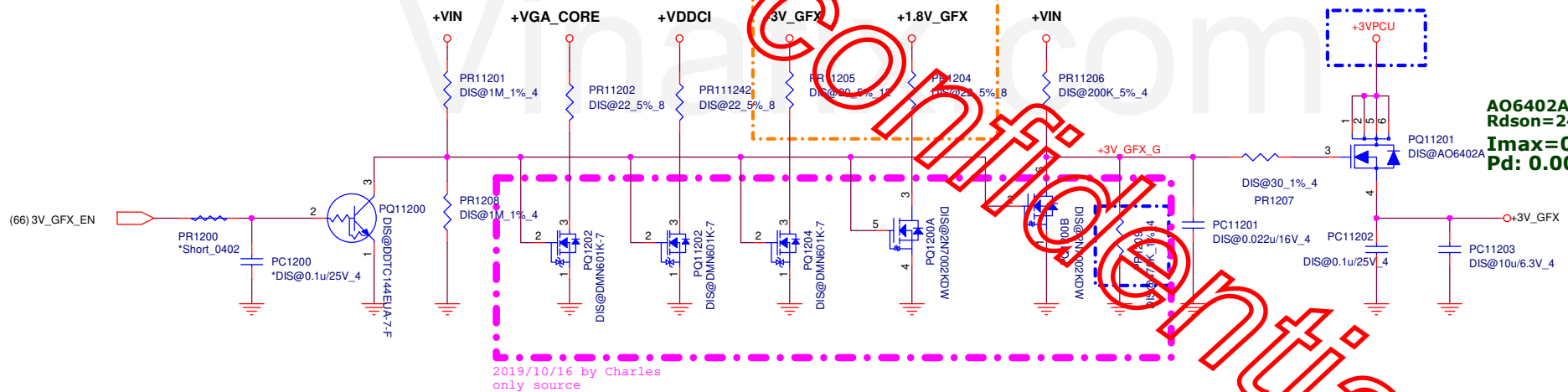
60mil
Max: 1A

+1.8V_GFX
I_{max} = 1 A
OCP = 4 A
Frequency = 1MHz
Ripple = 12mV
Delta IL = 0.8A

2019/6/14 by James Kuo

2019/05/09 by James Kuo
Per EE check result change to +3VPCU from +3VS5

AO6402A
R_{ds(on)} = 24m@10V V_{gs}
I_{max} = 0.01A
P_d = 0.003W

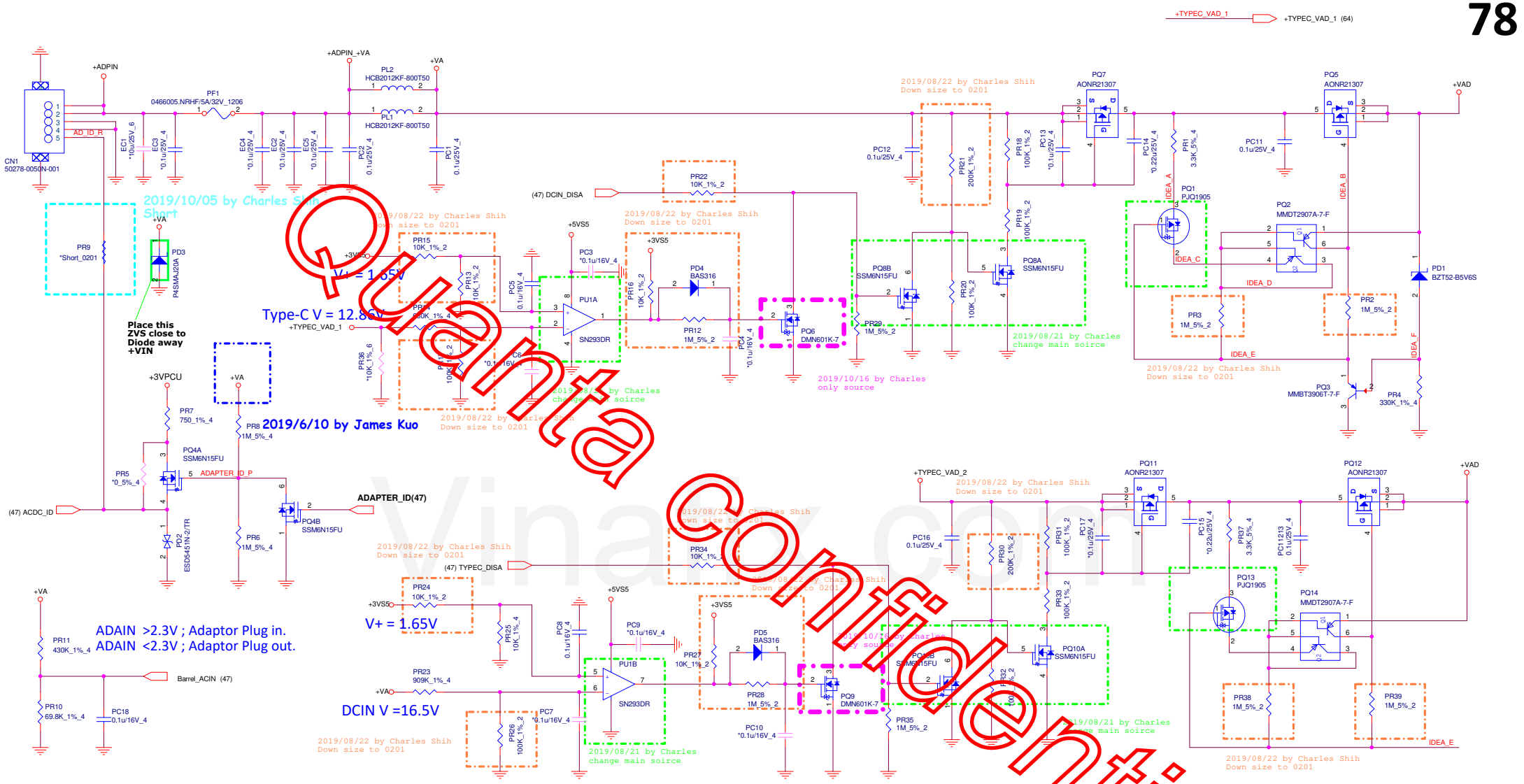


2019/10/16 by Charles
only source




PROJECT : LVC
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.8V_GFX(RT8068)/+3V_GFX	3A
Date:	Thursday, October 17, 2019	Sheet 77 of 91



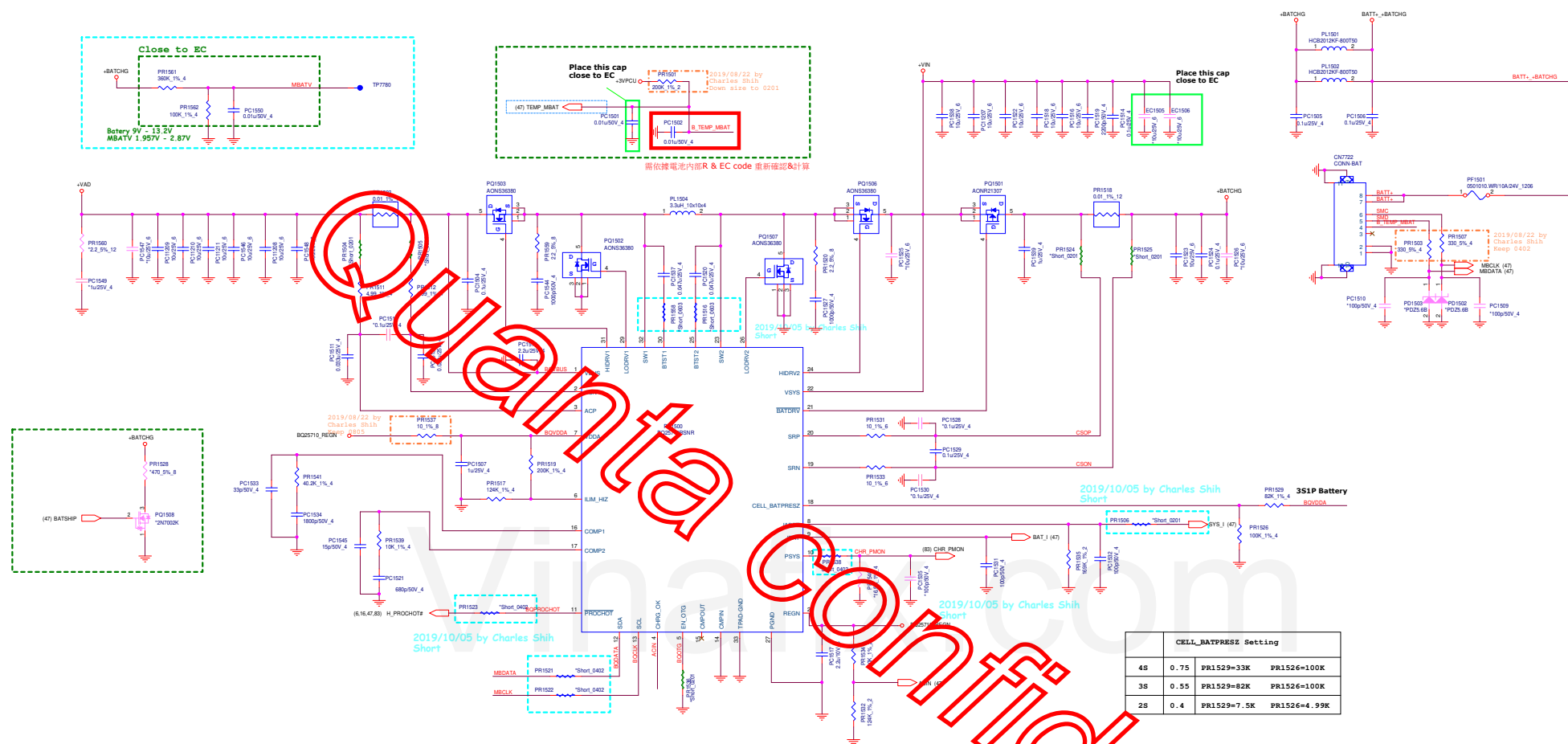
	TYPE C (95W) + Adaptor (65W)	TYPE C (65W) + Adaptor (65W)	TYPE C (45W) + Adaptor (65W)
DCIN_DISA (Default is Low)	High	Low	Low
TYPEPEC_DISA (Default is Low)	Low	High	High



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CELL_BATPREZ Setting			
4S	0.75	PR1529=33K	PR1526=100K
3S	0.55	PR1529=82K	PR1526=100K
2S	0.4	PR1529=7.5K	PR1526=4.99K

2019/05/9 by James Kuo
Change net name +3VPCU to +3V_ALW

2019/08/22 by Charles Shih
Down size to 0201

EE check

2019/10/05 by Charles Shih
Short

Do Not add test pad on LDO pin

Enable control. Pull this pin high to turn on the Buck. Do not leave this pin floating. EN pin will also be used to set USM mode, when EN pin voltage is between 0.8V and 1.7V, it will enter USM mode, if EN pin voltage is between 2.3V and 2.5V, then it is normal mode.

Part.	EN	VCC	VOUT	3.3V (LDO)	5V (LDO)
RT6258B	1	1	1	1	X
	0	1	0	1	X
RT6258C	1	1	1	X	1
	0	1	0	X	1

USB Charge support	Ra	Rb
(No support)	Stuff	NA
(Support)	NA	Stuff

Default setting

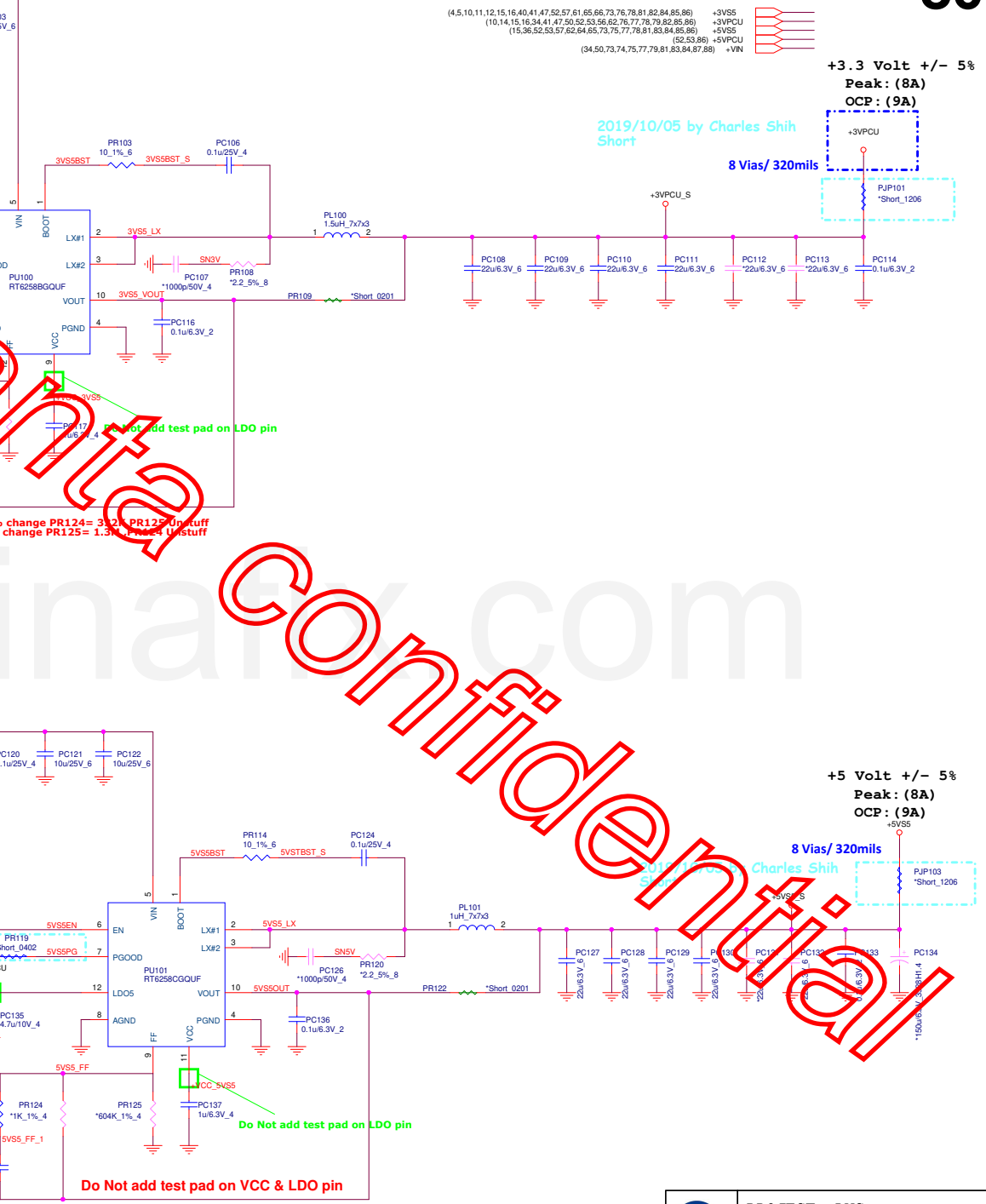
Normal mode
USM mode

Do Not add test pad on LDO pin

5 Vias/ 200mils

Do Not add test pad on VCC & LDO pin

SVSS +5% change R1= 604K R2 Unstuff
SVSS -5% change R1= 1.8M R2 Unstuff



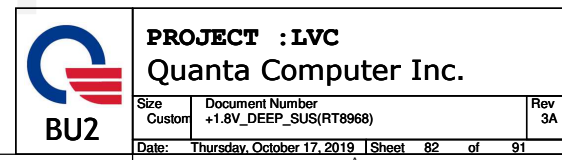
2019/10/05 by Charles Shih
Short

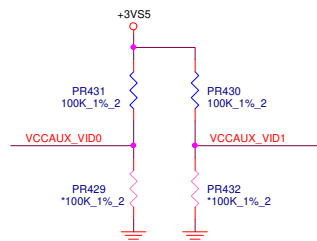
+3.3 Volt +/- 5%
Peak: (8A)
OCP: (9A)

8 Vias/ 320mils

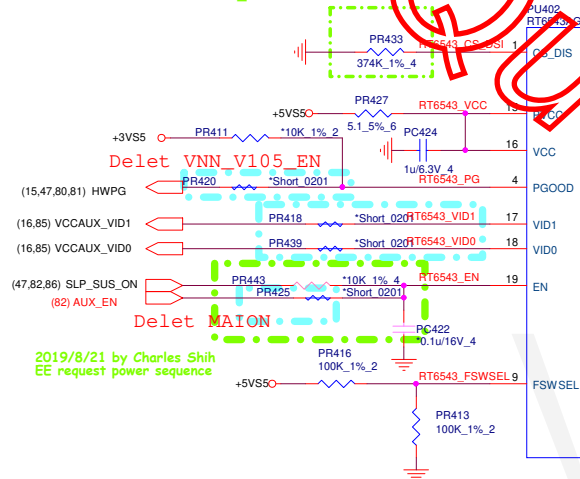
+5 Volt +/- 5%
Peak: (8A)
OCP: (9A)

8 Vias/ 320mils



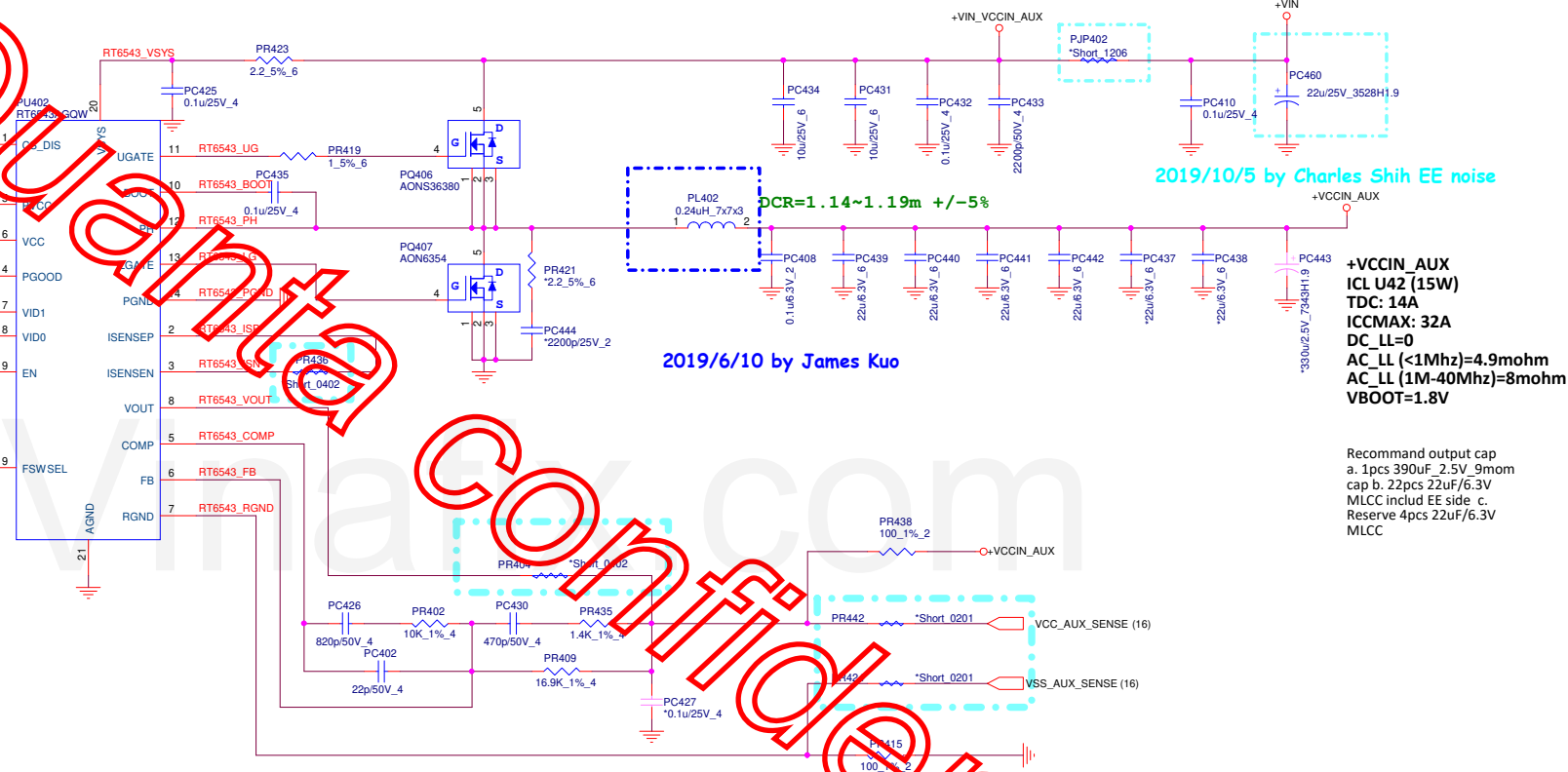


2019/8/21 by Charles Shih
VCCIN_AUX OCP



VID1	VID0	Vout
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

2019/7/26 by James Kuo

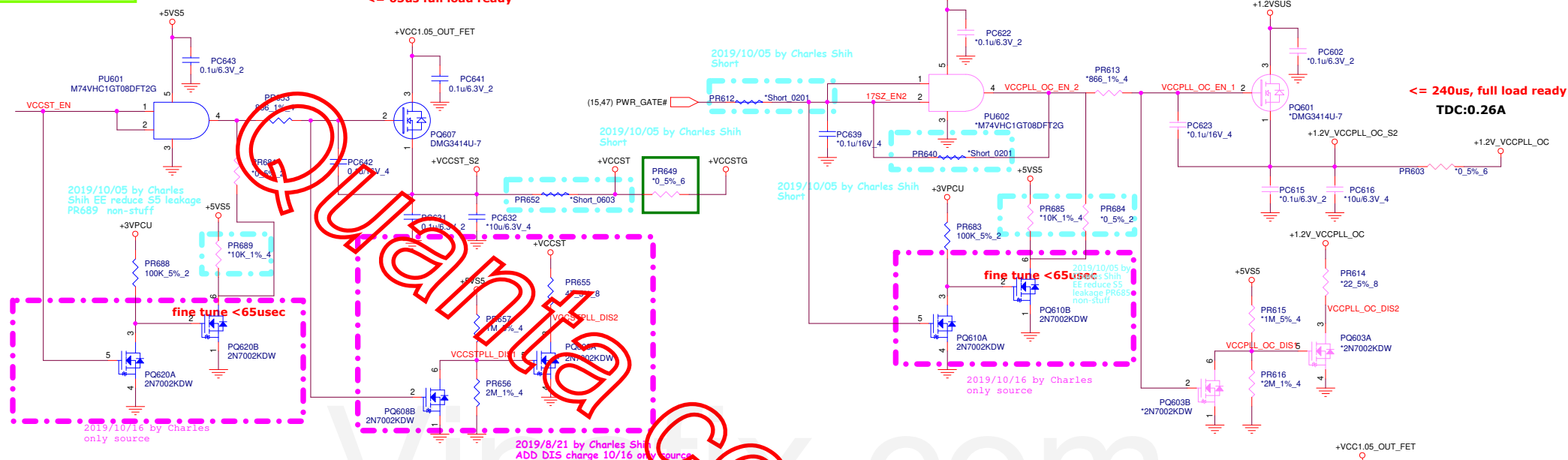


+VCCIN_AUX
ICL U42 (15W)
TDC: 14A
ICCMAX: 32A
DC_LL=0
AC_LL (<1Mhz)=4.9mohm
AC_LL (1M-40Mhz)=8mohm
VBOOT=1.8V

Recommend output cap
a. 1pcs 390uF_2.5V_9mohm
cap b. 22pcs 22uF/6.3V
MLCC includ EE side c.
Reserve 4pcs 22uF/6.3V
MLCC

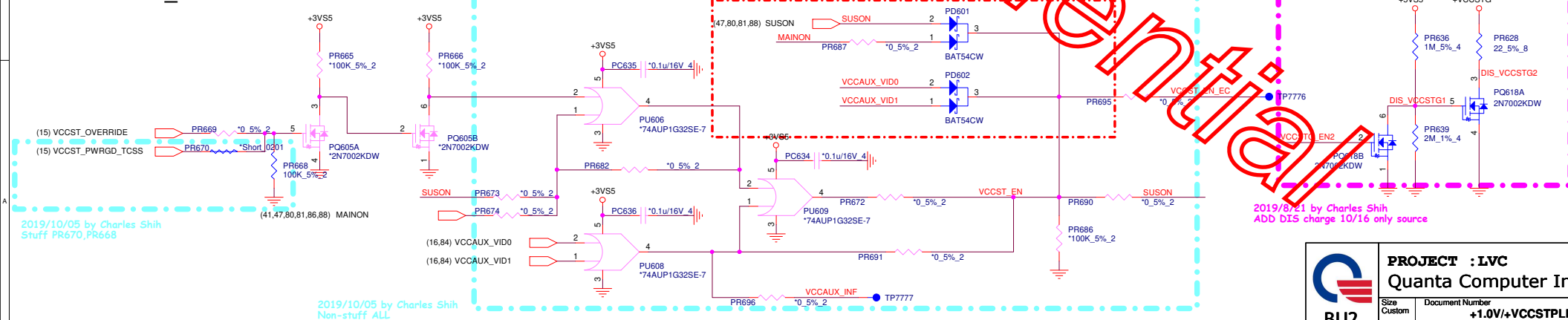
Volume Segment
ICL U42

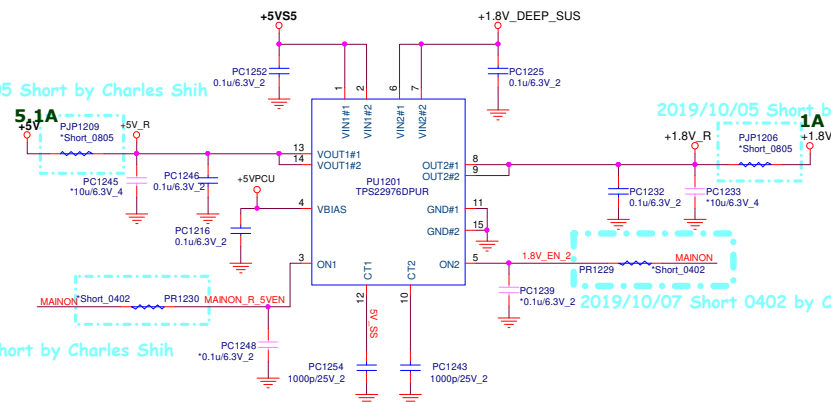
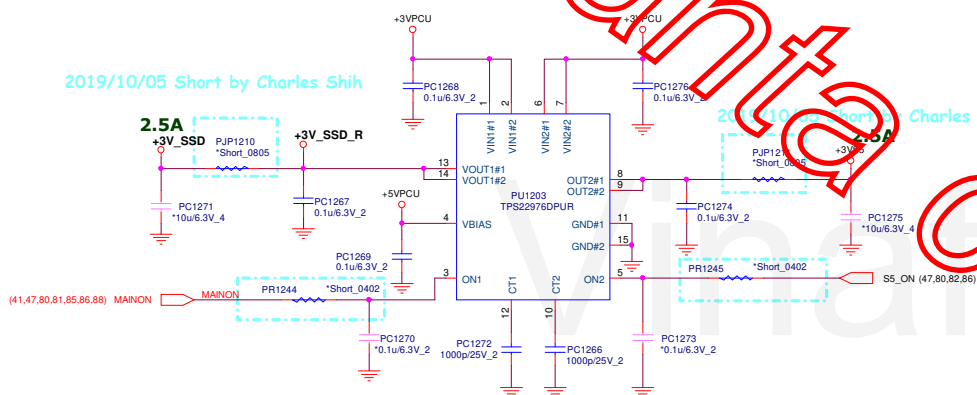
Volume Segment
VCCST: 0.65A
≤ 65us full load ready

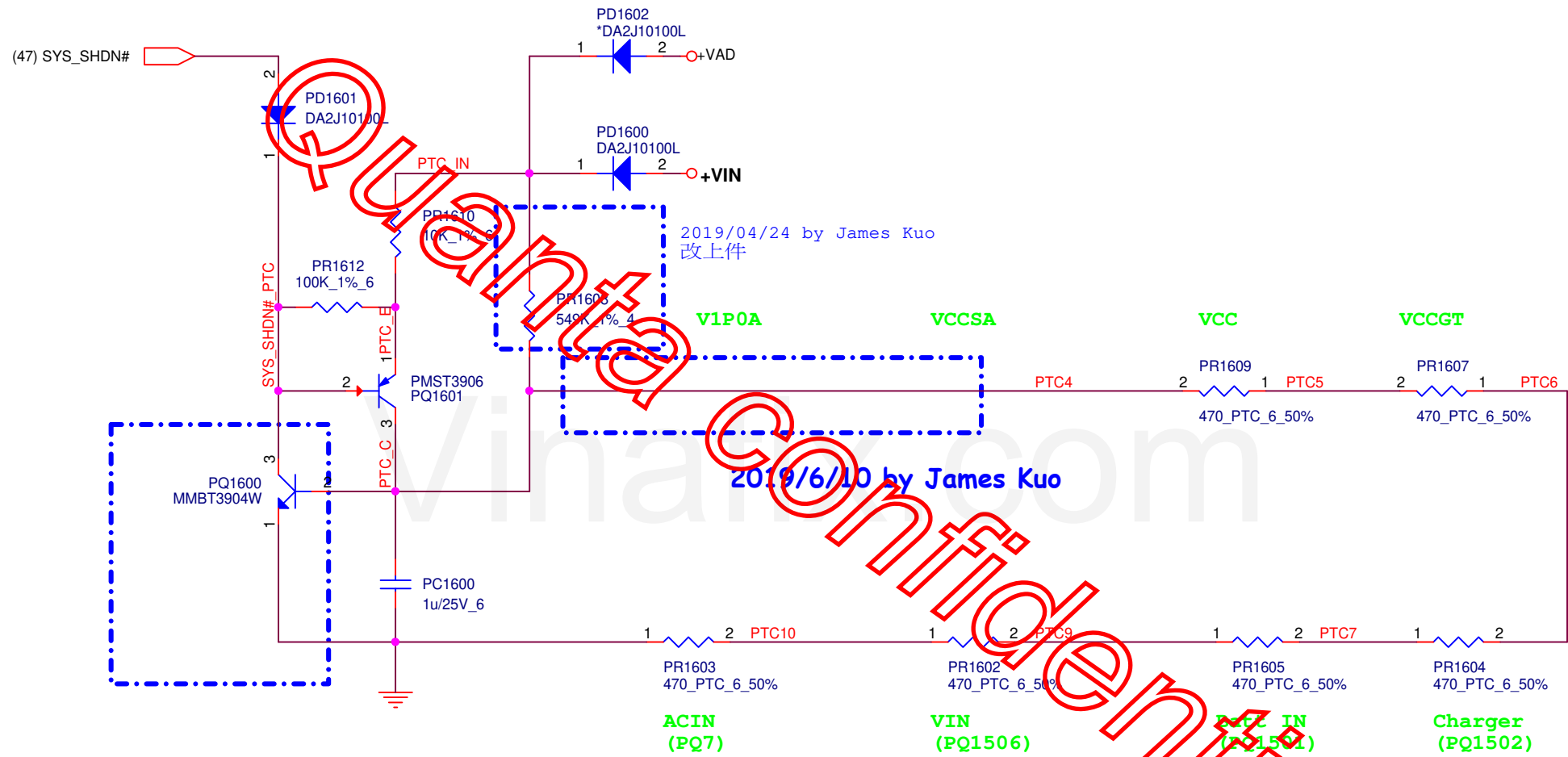


DOUBLE CHECK

VCCST_CPU GENERATION








2019/04/23 by James Kuo
PQ1600 change to BA039040019 from BA0390400B1

2019/04/24 by James Kuo
改上件

2019/6/10 by James Kuo

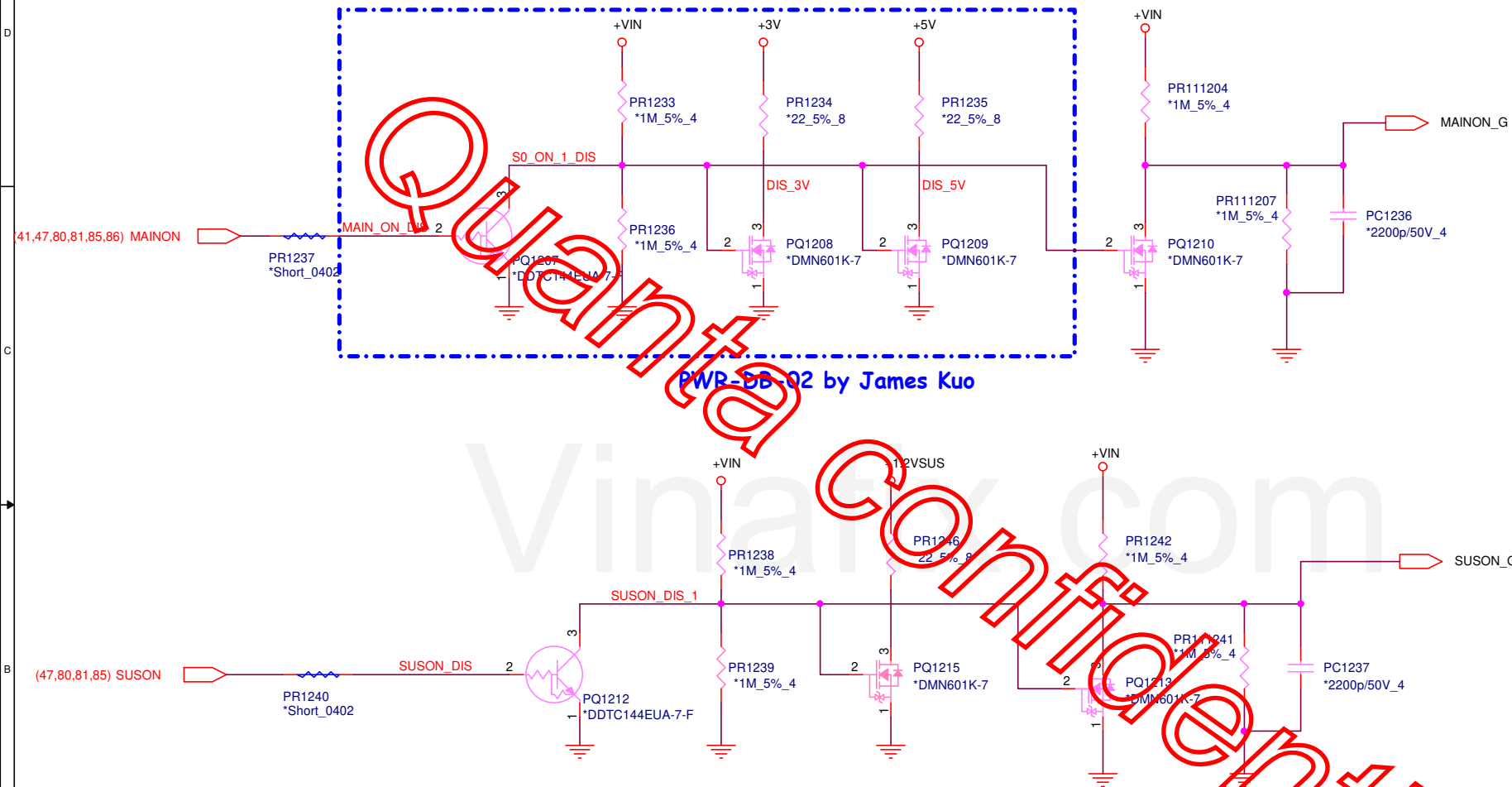


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Power rail discharge

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PWR-SB-02 by James Kuo

EC #	Page	Description	Part Affected
EC-DB-01	07	Add more caps for improving +VCCIN power quality	C28104,C28105,C28106,C28107,C28108,C28109,C28110,C28111
EC-DB-02	36	Codec vendor recommend to fix headphone GS-Mark test : Change r77810 and r77809 Res value from 10 ohm to 30 ohm	R77801,R77809
EC-DB-03	29	Intel recommend to fix s3 resume issue: change R1158 to 200 ohm and change R1163 to 604 ohm	R1158 , R1163
EC-DB-04	29	Intel recommend to fix s3 resume issue: change R1158 and R1163 to 1k ohm	R1158 , R1163
EC-SI-01	47	Fix boot-on issue(TOPSWAP) :unstuff R77880	R77880
EC-SI-02	47	To meet Intel Power sequence:unstuff R77981	R77981
EC-SI-03	13	To fix panel can not off when Lid close issue:add D6433 on PCH side	D6433
EC-SI-04	12	To correct GPIO table for bios setting	
EC-SI-05	07	Follow Intel CRB schematic:unstuff R701	R701
EC-SI-06	15	To fix ICL S3 resume issue and follow Intel CRB schematic: Add VCCST_PWGRD control circuit by SLP_S3	R77996,Q6434,Q6438,R78015,R78014,R78016
EC-SI-07	52	Fix ELAN Power rasing time issue:remove R power circuit	Add:R77909,R78001,Q6427,Q6428,C28112,C28113,C28114,R78000,R78009 Remove:R77913,R77914,R77909,U6414
EC-SI-08	43,53	Add reverse circuit to fix HDD LED issue	Add:R77994,Q6424,R77969
EC-SI-09	56	Remodify BIOS ROM power circuit	D6434,R77964,R77999,D6435
EC-SI-10	05	Reserve pull down R78002 for DDR_VTT_CTRL	R78002
EC-SI-11	61	Fix Type-C DP no display when S3 resume to S0 and chang Type-C mux power to +5V3 power stand	Unstuff:Q6409,R28049,C8681,L7607 stuff:L7627,L7628
EC-SI-12	14	Add RTC current limiter resistance for Safety recommend	R77988
EC-SI-13	57,65	Follow V340 CML USB3.1 common choke design	Change BOM:R77914,R7623 removed:R7623,L7624,L7625,L7626
EC-SI-14	47	To prevent PM_THRMTRIP# glitch when power-on:add pull high +VCCSTG circuit to collector-base of Q4701	R78003
EC-SI-15	53	Reserve power rail "+3VPCU" for battery LED	R78004,R78005
EC-SI-16	41,43,44	Add current sense to measure power consumption	R78007,R77985,R78007
EC-SI-17	34	Reduce Power ripple for +LCD_VDD and +CCD_VDD:add more capacitances	C28121,C28115,C28116,C28113,C28118,C28119
EC-SI-18	61,65	Reduce usb2 layout stub: add more resistance	R78010,R78011,R78012,R78013
EC-SI-19	62	To prevent VCON_IN_1 voltage drop:reserve power switch circuit	U28024,C28123,C28124
EC-SI-20	53	Fine tune LED brightness:change current limiter resistance to 680 ohm	R3700/R3701/R3702
EC-SI-21	66	Fine tune GPU power sequence:change R2284 to 17.4k	R2284
EC-SI-22	47	To prevent PM_THRMTRIP# glitch when power-on:unstuff R78003	R78003
EC-PV-01		Change 0 ohm to shortpad for company policy	R77916,R77915,R77951,R780,R702,R705,R706,R707,R1613,R1618, R1601,R1600,R1615,R1606,R3617,R77971,R77972,R77973,L3605, R77919,R5314,R5302,R78009,R77906,R77907,R78004,R77964, R77840,R77841,R77842,R77843,R77844,R77845,R77846,R77839 R77831,R77832,R77833,R77834,R77835,R77836,R77837,R77838 R77871,R77872,R2086,R77815,R77816,R28066,L4701,L4700,R2194 R506,R609,R610,R612,R613,R615,R1105,R1416,R1419,R1420 R77937,R1528,R77918,R78014,R78015,R1527,R1520,R1604,R1605 R4765,R77968,R77979,R8636,R77986,R77987,R77988, R77989,R77990,R77991,R77992,R77993,R77976,R77975 R700,R1614,R77947,R77808,R77807,R77811,R77812 R224,R77985,R78007,R78008,PJP1702
EC-PV-02	52	Lenovo recommend to reserve finger print SSO function	R78025,R78026,R78024,R78022,R78023
EC-PV-03	57	RF recommend to change type-A RF choke	L7621,L7622
EC-PV-04	07,16	Reduce RF noise and add more caps on power treace of +VCCIN_AUX/+VCCIN downsize C712 to c0201 due to layout space	C28126,C28127,C28128,C28129,C28130,C28131,C28132,C28133 C28134,C28135,C28136,C28137,C28138,C28139,C28140,C28141 C712
EC-PV-05	04	remove useless resistances	R77915,R77916
EC-PV-06	12	Correct GPIO table	R1553,R1554,R1555
EC-PV-07	15	follow intel design guide and pull high circuit for PMCALERT#	R78017
EC-PV-08	41,47,53, 62	change and unstuff BOM to reduce AC S5 leakage	R4102,R78021,R4708,R4759,R77883,R77965,Q33,Q34
EC-PV-09	57	correct current limit setting and re-modify AOU CTL pull high to +5VS5	R7829,R28037,R28038,R78018,R7828,R78019

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